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DISPLAY TECHNOLOGY

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Datasheet

KOE

TX26D208VM0AAA

10.2" TFT

KO-01-004

KOE

JDI Group

TENTATIVE

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____

DATE : May 08th ,2020

TECHNICAL DATA

TX26D208VM0AAA

Contents

ACCEPTED BY: _____

PROPOSED BY: John Chou

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY
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3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 10.2” FHD of 16:9 format of LTPS TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX26D208VM0AAA
Module Dimensions	241.9 (W) mm x 147. 8(H) mm x 12.6 (D) mm
LCD Active Area	225.792 (W) mm x 127.008(H) mm
Pixel Pitch	0.1176(W) mm x 0.1176 (H) mm
Resolution	1920 x 3(RGB)(W) x 1080(H) dots
Color Pixel Arrangement	R, G, B Vertical Stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	16.7M Colors(8 bit RGB)
Backlight	Light Emitting Diode (LED)
Weight	415g
Interface	2ch-LVDS; 50 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	LCD (0.56)W ; BL (10)W
Viewing Direction	Super Wide Version (In-Plane Switching)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.2	4.0	V	-
Input Voltage of Logic	V_I	-0.2	V_{DD} +0.3	V	Note 1
Operating Temperature	T_{op}	-40	85	°C	Note 2
Storage Temperature	T_{st}	-40	90	°C	Note 2
Backlight Input Voltage	V_{LED}	-0.3	20	V	-
Backlight Voltage for PWM	V_{PWM}	-0.3	5	V	-
Backlight Voltage for EN	V_{EN}	-0.3	5	V	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the glass surface temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 DC CHARACTERISTICS OF GENERAL

$T_a = 25\ ^{\circ}C,\ \mathrm{GND} = 0\mathrm{V}$

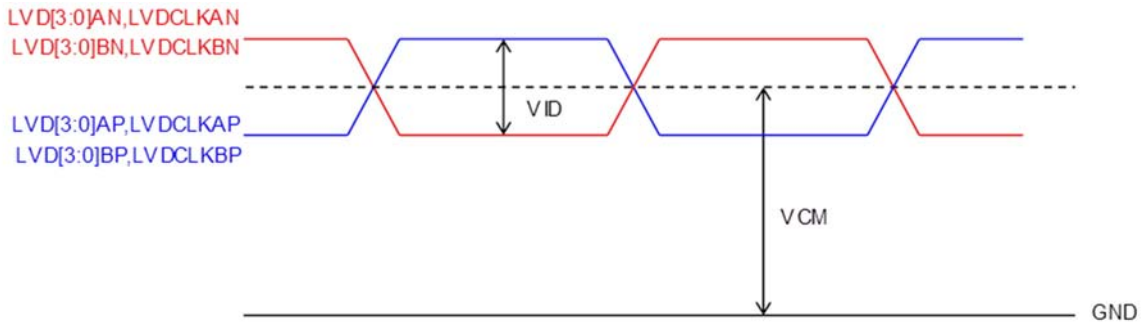
Item	Symbol	Condition	Standard Value			Unit	Remarks
			Min.	Typ.	Max.		
Power supply voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Power supply current	I_{DD}	Note 1	-	(170)	-	mA	Note 1,5
Input signal voltage	V_{IH}	-	$0.7V_{DD}$	-	V_{DD}	V	Note 2
	V_{IL}	-	V_{SS}	-	0.5	V	
Allowable Ripple Voltage	VRP	-	-	-	50	mV (p-p)	Note 3
Differential Input High Threshold	VTH	VICM=1.25V	-	-	100	mV	Note 4
Differential Input Low Threshold	VTL	VICM=1.25V	-100	-	-	mV	
Input Differential Voltage	|VID|	-	350	450	600	mV	
Differential Input Common Mode Voltage	VCM	-	1.0	1.25	1.5	V	
Termination resistor	RTRM		95	100	105	ohm	

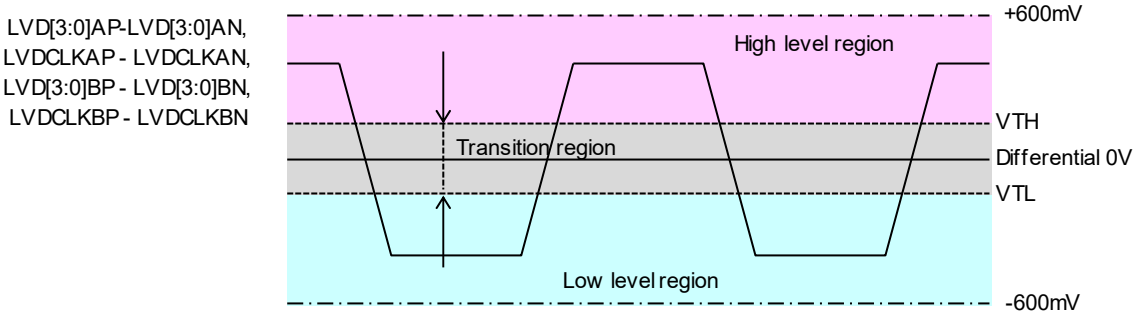
Note 1: An all white check pattern is used when measuring I_{DD} frame rate is set to 60Hz with Typ voltage.

Note 2: Applied pin is {UD , LR, ON/OFF }.

Note 3: Applied pin is {V_{DD}}

Note 4: For LVDS input signal.





Note 5: (2A) fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than (5A) to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	I_{LED}=(840)mA	10.8	12	13.2	V	Note 1
LED Forward Current	I_{LED}	100% duty	-	(840)	-	mA	Note 2
		0% duty	-	(3)	-		
PWM Signal Voltage	V_{pwm}	High	2	-	3.6	V	-
		Low	-	-	0.8		
EN Voltage	V_{EN}	-	2	-	3.6	V	-
LED Lifetime	-	I_{LED}=(840)mA	-	70K	-	hrs	Note 3

Note 1: Fig. 5.1 shows the LED backlight circuit.

Note 2: Dimming function can be obtained by applying PWM signal from the display interface CN2. The recommended PWM signal is 200Hz ~ 1KHz with 3.3 V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying (840)mA at 25°C.

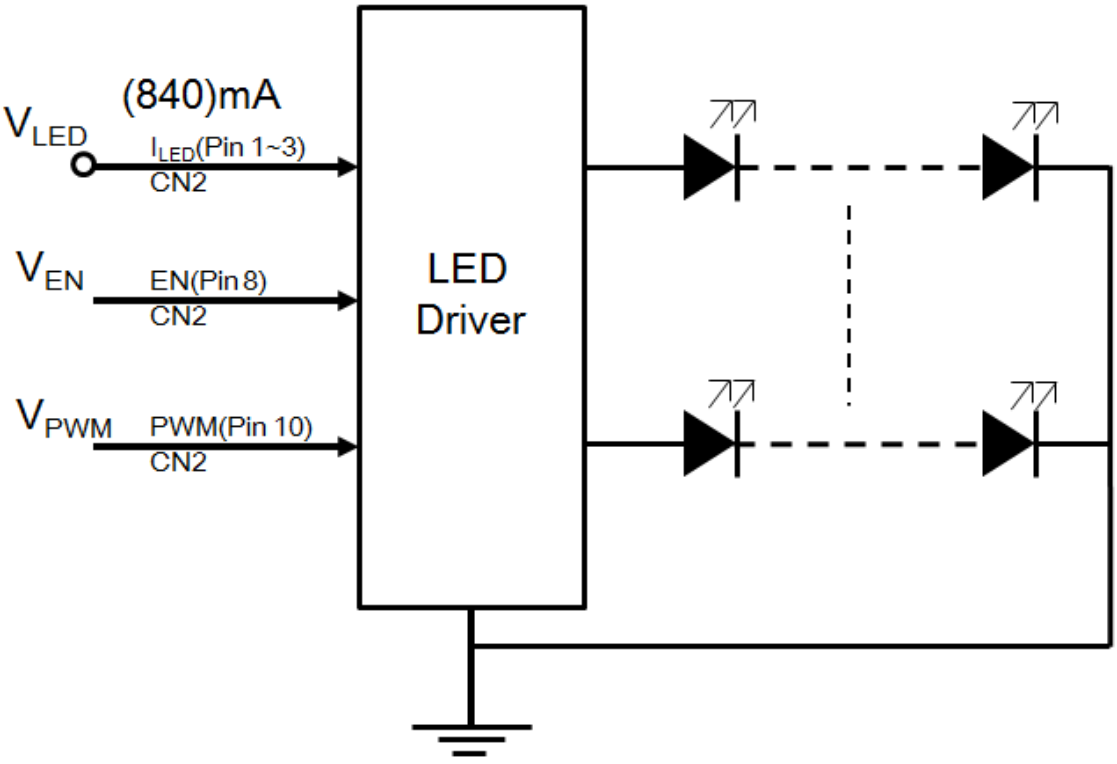


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C,\ f_{Frame} = 60\,\text{Hz}, V_{DD} = 3.3\text{V}$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, I_{LED}= (840) mA	-	1200	-	cd/m^2	Note 1
Brightness Uniformity		-		-	-	-	%	Note 2
Contrast Ratio		CR		-	1000	-	-	Note 3
Response Time		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	25	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	72	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	-	85	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	-	85	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	-	85	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	-	85	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	(TBD)	-	-	Note 6
		Y		-	(TBD)	-		
	Green	X		-	(TBD)	-		
		Y		-	(TBD)	-		
	Blue	X		-	(TBD)	-		
		Y		-	(TBD)	-		
	White	X		-	(TBD)	-		
		Y		-	(TBD)	-		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \text{ X100\%}$$

which is based on the brightness values of the 9 points in active area measured by BM-5 as shown in Fig. 6.2.

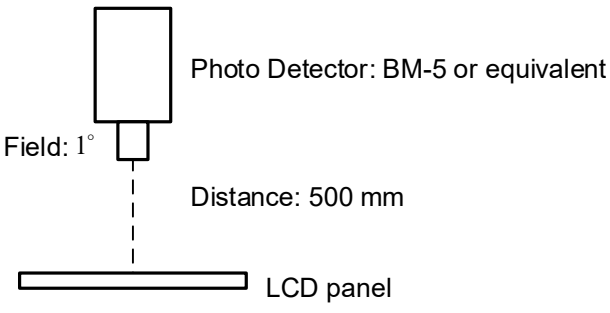


Fig 6.1

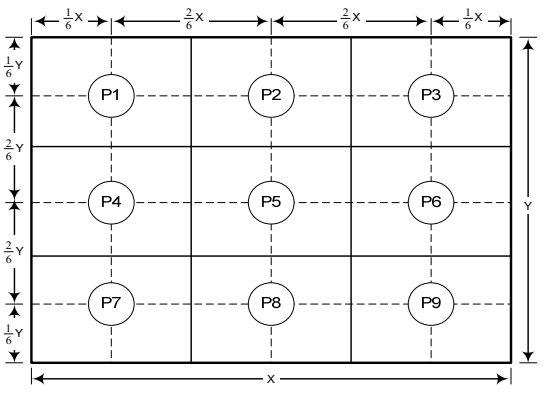


Fig 6.2

Note 3: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.

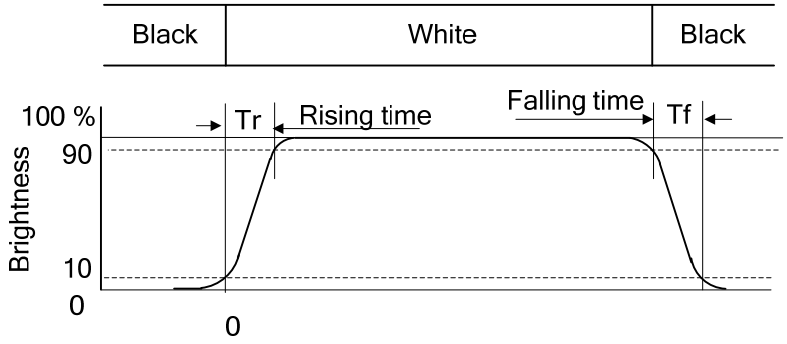


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version; 85° viewing angle can be obtained from each viewing direction.

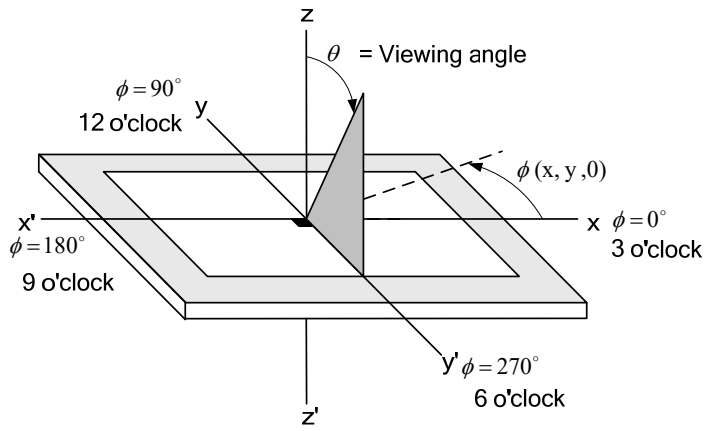
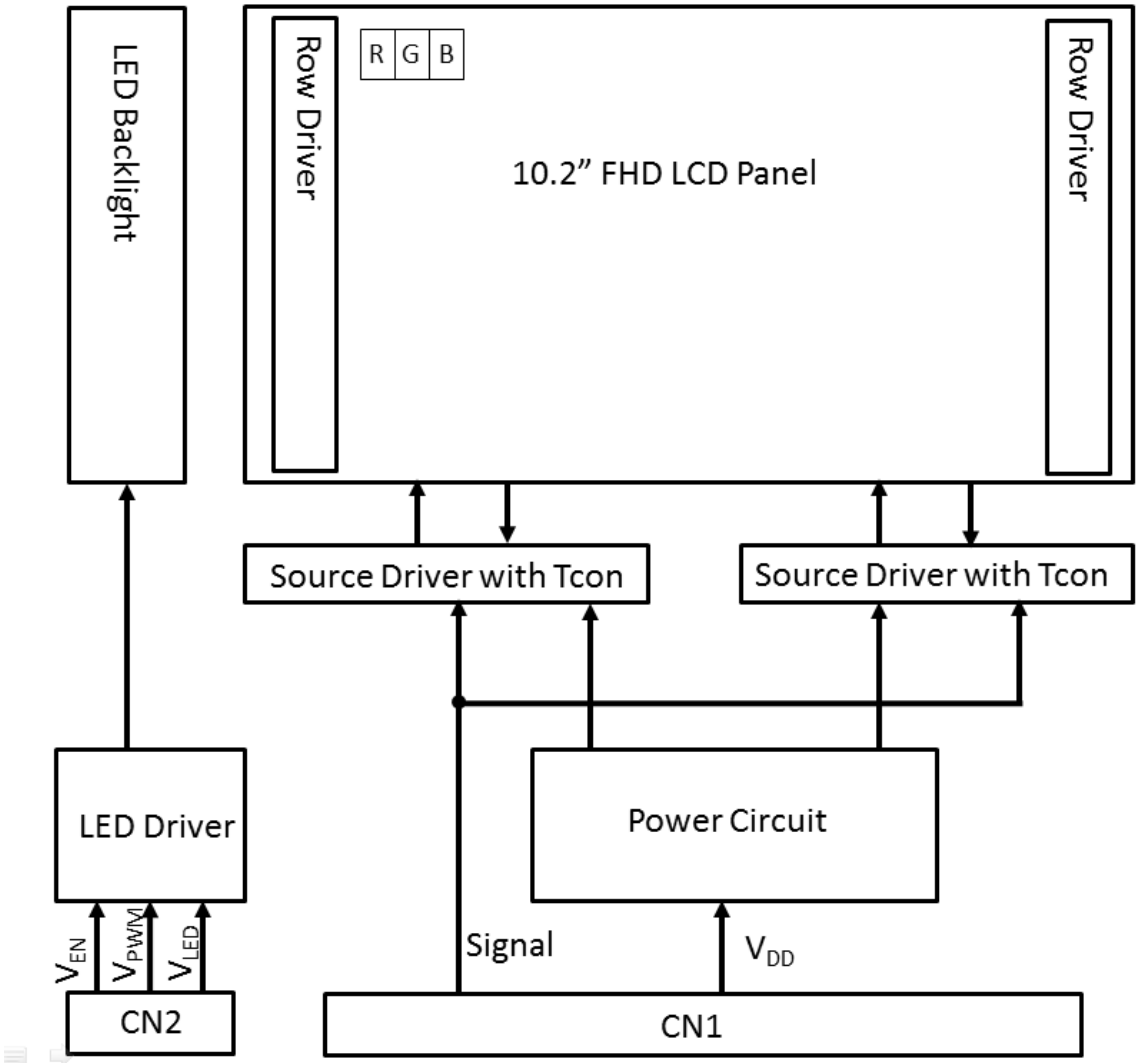


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note 1: Signals are CLK and pixel data pairs.

8. LCD INTERFACE

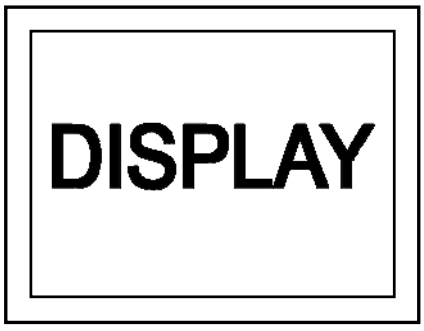
8.1 INTERFACE PIN CONNECTIONS

The display interface connector CN1 is FH28-50S-0.5SH (Hirose), and Pin assignment is as below:

No.	Signal	Signal	I/O/P	Note
1	NC	No connect	I	
2	NC	No connect	I	
3	NC	No connect	I	
4	NC	No connect	I	
5	LR	Horizontal display mode control	I	Note 1
6	UD	Vertical display mode control	I	Note 1
7	GND	GND	P	
8	GND	GND	P	
9	GND	GND	P	
10	GND	GND	P	
11	NC	No connect	P	
12	V_{DD}	Power supply for LCD	P	
13	V_{DD}	Power supply for LCD	I	
14	NC	No connect	I	
15	NC	No connect	P	
16	NC	No connect	P	
17	NC	No connect	I	
18	GND	GND	P	
19	ON/OFF	Display on/off	I	
20	GND	GND	I	
21	LVD0AN	(LVDS) A-port LVDS data0 (negative)	I	
22	LVD0AP	(LVDS) A-port LVDS data0 (positive)	I	
23	GND	GND	P	
24	LVD1AN	(LVDS) A-port LVDS data1 (negative)	I	
25	LVD1AP	(LVDS) A-port LVDS data1 (positive)	I	

No.	Signal	Signal	I/O/P	Note
26	GND	GND	P	
27	LVD2AN	(LVDS) A-port LVDS data2 (negative)	I	
28	LVD2AP	(LVDS) A-port LVDS data2 (positive)	I	
29	GND	GND	P	
30	LVCLKAN	(LVDS) A-port LVDS CLK (positive)	I	
31	LVCLKAP	(LVDS) A-port LVDS CLK (negative)	I	
32	GND	GND	P	
33	LVD3AN	(LVDS) A-port LVDS data3 (negative)	I	
34	LVD3AP	(LVDS) A-port LVDS data3 (positive)	I	
35	GND	GND	P	
36	LVD0BN	(LVDS) B-port LVDS data0 (negative)	I	
37	LVD0BP	(LVDS) B-port LVDS data0 (positive)	I	
38	GND	GND	P	
39	LVD1BN	(LVDS) B-port LVDS data1 (negative)	I	
40	LVD1BP	(LVDS) B-port LVDS data1 (positive)	I	
41	GND	GND	P	
42	LVD2BN	(LVDS) B-port LVDS data2 (negative)	I	
43	LVD2BP	(LVDS) B-port LVDS data2 (positive)	I	
44	GND	GND	P	
45	LVCLKBN	(LVDS) B-port LVDS CLK (positive)	I	
46	LVCLKBP	(LVDS) B-port LVDS CLK (negative)	I	
47	GND	GND	P	
48	LVD3BN	(LVDS) B-port LVDS data3 (negative)	I	
49	LVD3BP	(LVDS) B-port LVDS data3 (positive)	I	
50	GND	GND	P	

Note 1: Scan direction is available to be switched as below.



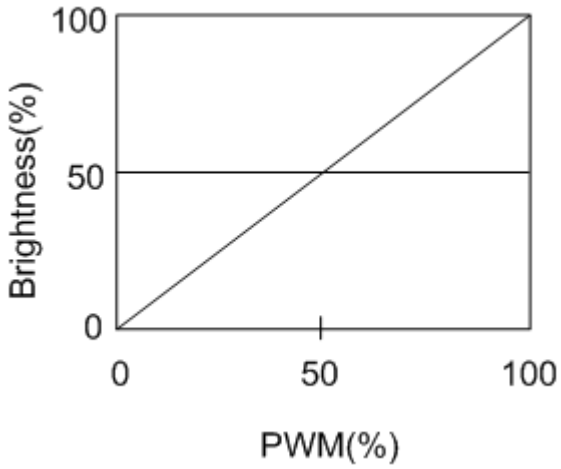
LR：H or Open
UD：L or Open

LR：L
UD：H

The interface CN2 is SM10B-SRSS-TB(LF)(SN) made by JST and pin assignment is as below:

Connector Name	Pin No.	Symbol	Function
SM10B-SRSS-TB(LF)(SN)	1	V_{LED}(+)	Power Supply for LED
	2	V_{LED}(+)	Power Supply for LED
	3	V_{LED}(+)	Power Supply for LED
	4	NC	No Connection
	5	V_{LED}(-)	GND
	6	V_{LED}(-)	GND
	7	V_{LED}(-)	GND
	8	V_{EN}	Backlight Enable
	9	NC	No Connected
	10	V_{PWM}	Brightness dimming

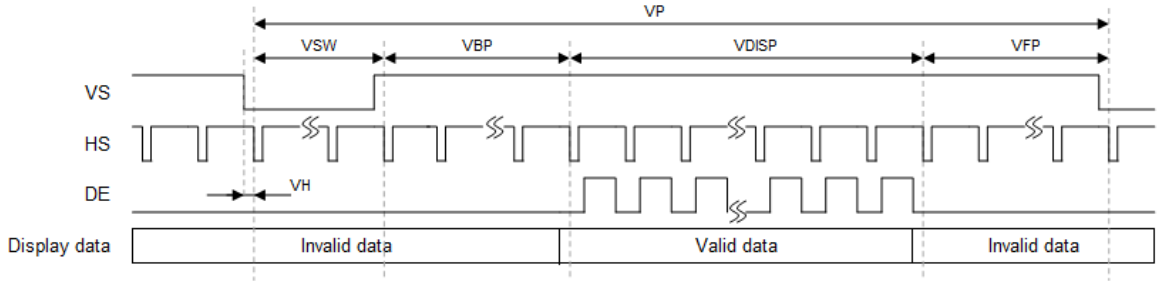
Note 1: The relationship of brightness and Dim control are shown as below.



Note 2: Normal brightness : 100% PWM duty ; Brightness control : 0% to 100% PWM duty. If no using , please keep it high(100%).

8.2 Data Input Timing

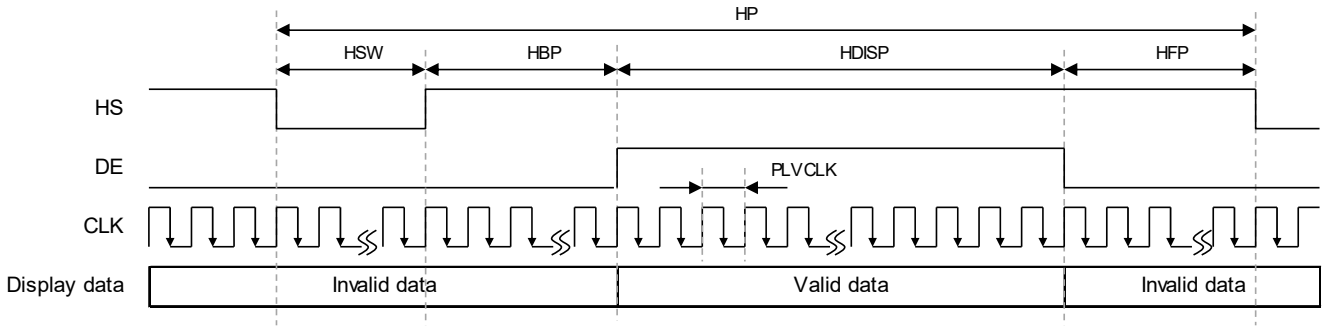
(1) Vertical timing



Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
VP	Vertical cycle	1095	1095	1095	Line	
VSW	Vertical “L” period	1	5	10	Line	
VBP	Vertical back porch	1	5	10	Line	
VFP	Vertical front porch	4	5	10	Line	
VDISP	Vertical active area	1080	1080	1080	Line	
VSW+VBP+VFP	Vertical porch	15	15	15	Line	
VRR	Frame rate	59.41	60.01	60.61	Hz	

Note : In case of changing the vertical and horizontal timing, the display should be turned off.

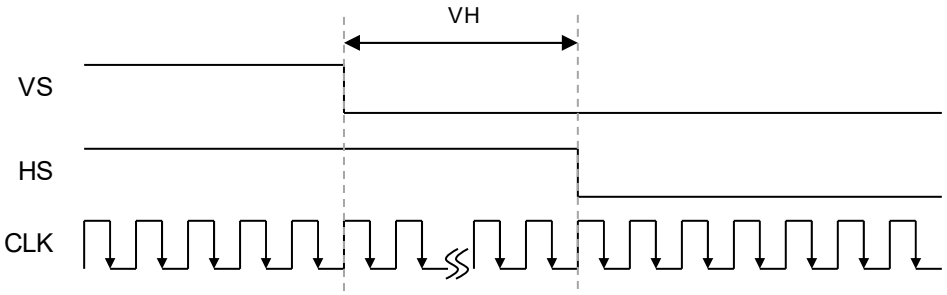
(2) Horizontal timing



Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
HP	Horizontal cycle	1130	1130	1130	LVCLK	
HSW	Horizontal “L” width	10	40	140	LVCLK	
HBP	Horizontal back porch	10	50	140	LVCLK	
HFP	Horizontal front porch	20	80	130	LVCLK	
HDISP	Horizontal active area	960	960	960	LVCLK	
HSW+HBP+HFP	Horizontal porch	170	170	170	LVCLK	
f_{LVCLK}	Pixel clock frequency	73.51	74.25	74.99	MHz	
PLVCLK		13.33	13.47	13.60	ns	

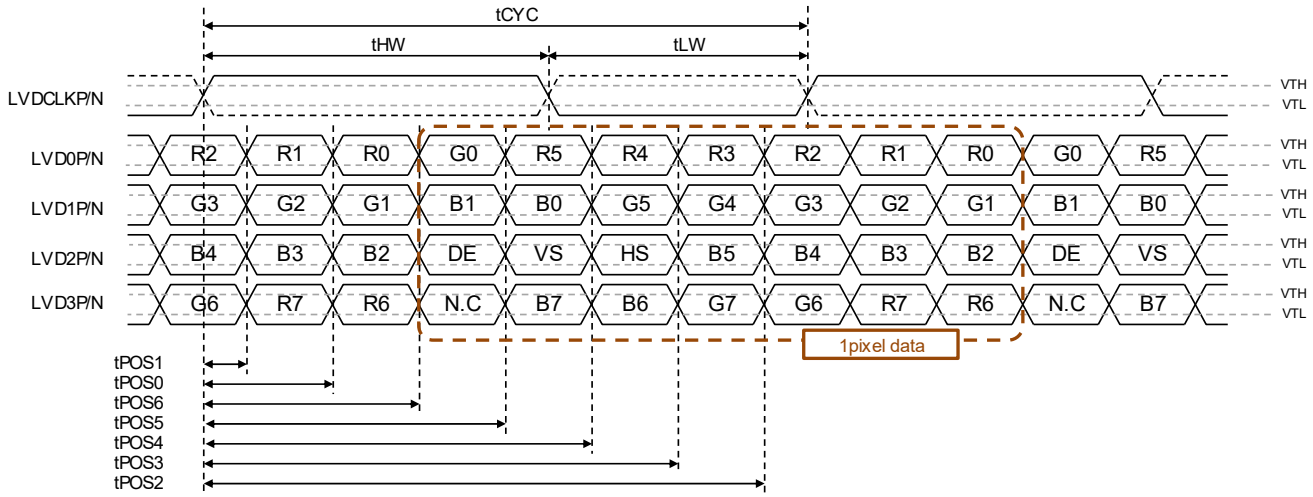
Note : In case of changing the vertical and horizontal timing, the display should be turned off.

(3) VS – HS timing

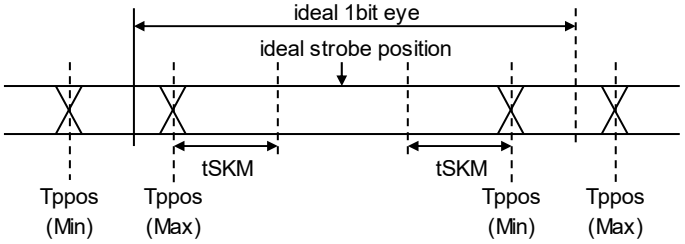


Symbol	Item	Min.	Typ.	Max.	Unit	Remarks
VH	Phase difference of VS-HS	0	0	0	LVCLK	

8.3 LVDS AC TIMING

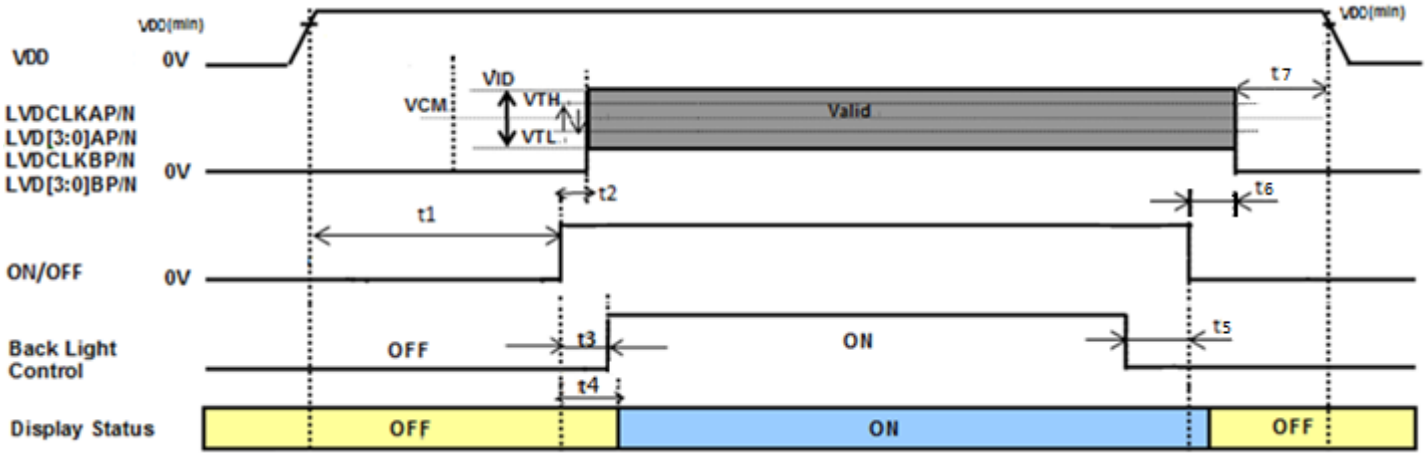


Note 1: above timing chart is based on LVDS Format VESA.



Signal	Symbol	Item	Min.	Typ.	Max.	Unit
LVDCLKAP/N LVDCLKBP/N	tCYC	clock cycle time	13.33	13.47	13.60	MHz
			0.4 x tCYC	0.5 x tCYC	0.6 x tCYC	ns
	tHW	clock "H" pulse width	0.4 x tCYC	0.5 x tCYC	0.6 x tCYC	ns
	tLW	clock "L" pulse width	(-4/7)	0	(4/7)	ns
LVD[3:0]AP/N LVD[3:0]BP/N	tPOS1	tPOS1 position	- tSKM	0	+ tSKM	ns
	tPOS0	tPOS0 position	(1/7)x tCYC - tSKM	(1/7)x tCYC	(1/7)x tCYC + tSKM	ns
	tPOS6	tPOS6 position	(2/7)x tCYC - tSKM	(2/7)x tCYC	(2/7)x tCYC + tSKM	ns
	tPOS5	tPOS5 position	(3/7)x tCYC - tSKM	(3/7)x tCYC	(3/7)x tCYC + tSKM	ns
	tPOS4	tPOS4 position	(4/7)x tCYC - tSKM	(4/7)x tCYC	(4/7)x tCYC + tSKM	ns
	tPOS3	tPOS3 position	(5/7)x tCYC - tSKM	(5/7)x tCYC	(5/7)x tCYC + tSKM	ns
	tPOS2	tPOS2 position	(6/7)x tCYC - tSKM	(6/7)x tCYC	(6/7)x tCYC + tSKM	ns
	tSKM	Skew margin	-	-	(300)	ps

8.6 POWER ON / OFF SEQUENCE

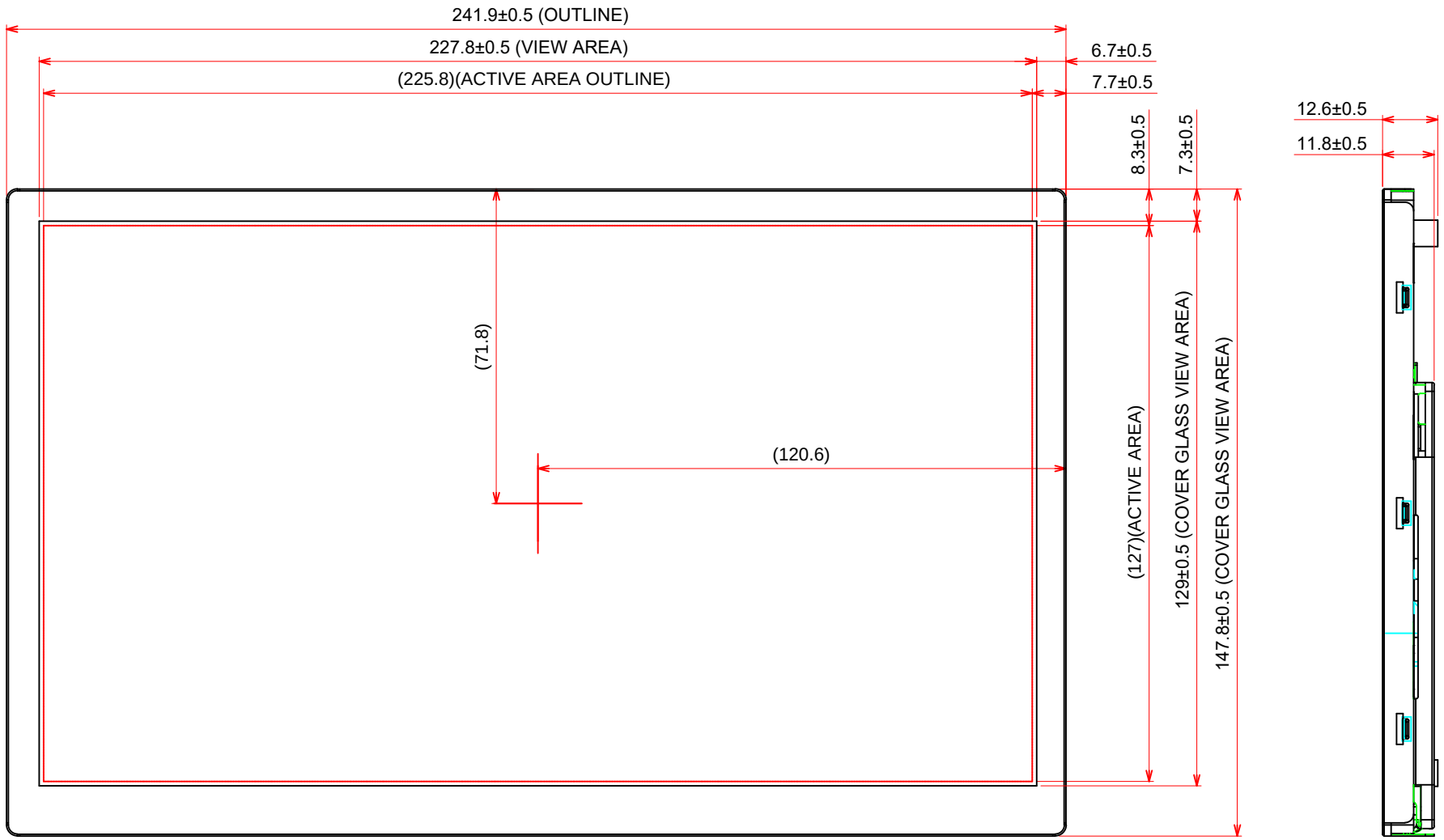


Please design the circuit which is able to adjust the interval of following table.

	‘t1	‘t2	‘t3	‘t4	‘t5	‘t6	‘t7
Min.	(0ms)	(10ms)	(135ms)	(-)	(0ms)	(200ms)	(0ms)
Max.	(-)	(-)	(-)	(150ms)	(-)	(-)	(-)

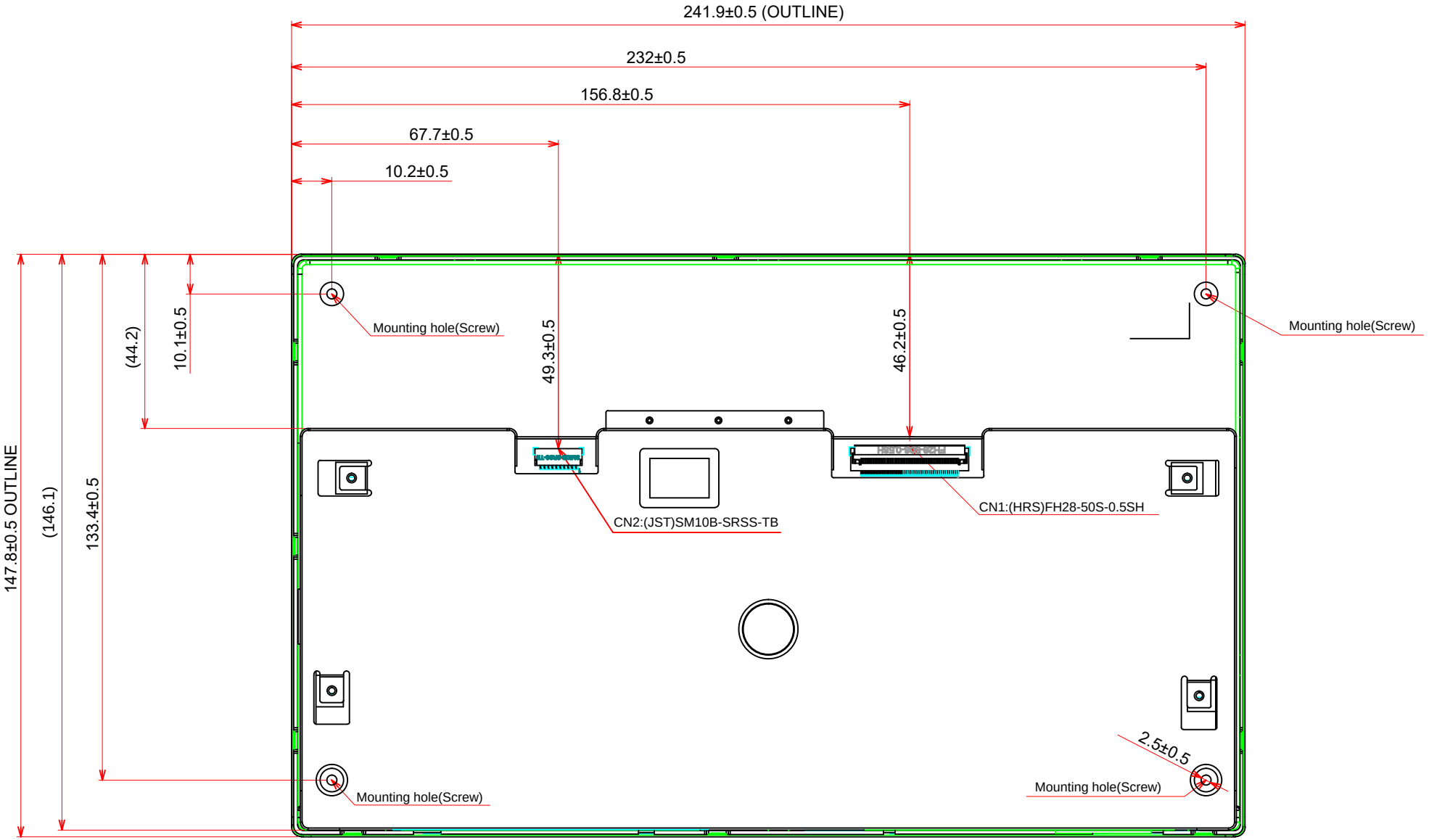
9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

9.2 RAER VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

KAOHSIUNG OPTO-ELECTRONICS INC.	SHEET No.	7B64LTD-2627-2	PAGE	9-2/2

10. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.10.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

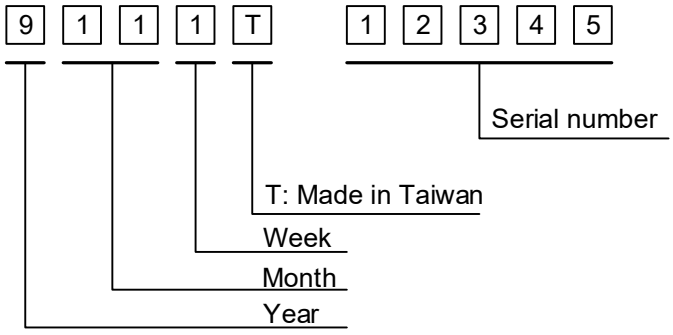


Fig. 10.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2019	9
2020	0
2021	1
2022	2
2023	3

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) The location of the lot mark is on the back of the display shown in Fig. 10.2

Label example:

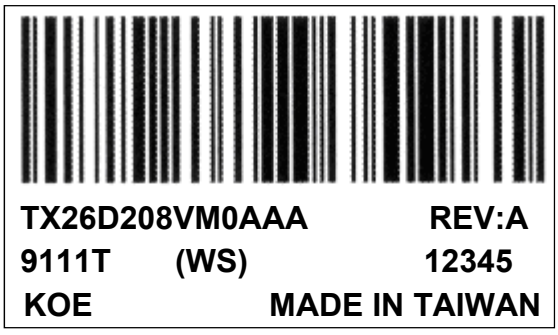


Fig. 10.2

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

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