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Datasheet

Disea

ZW-T080QYH-01

DE-05-013

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Disea Electronics Co., LTD

PRODUCT SPECIFICATIONS

For Customer: _____ ☐ : APPROVAL FOR SPECIFICATION

Customer Model No. _____ ☐ : APPROVAL FOR SAMPLE

Module No.: ZW-T080QYH-01 Date : 2016-07-01

Table of Contents

For Customer's Acceptance:

Approved By	Comment

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT
mma	john		Dmjiang

2. Revision Record

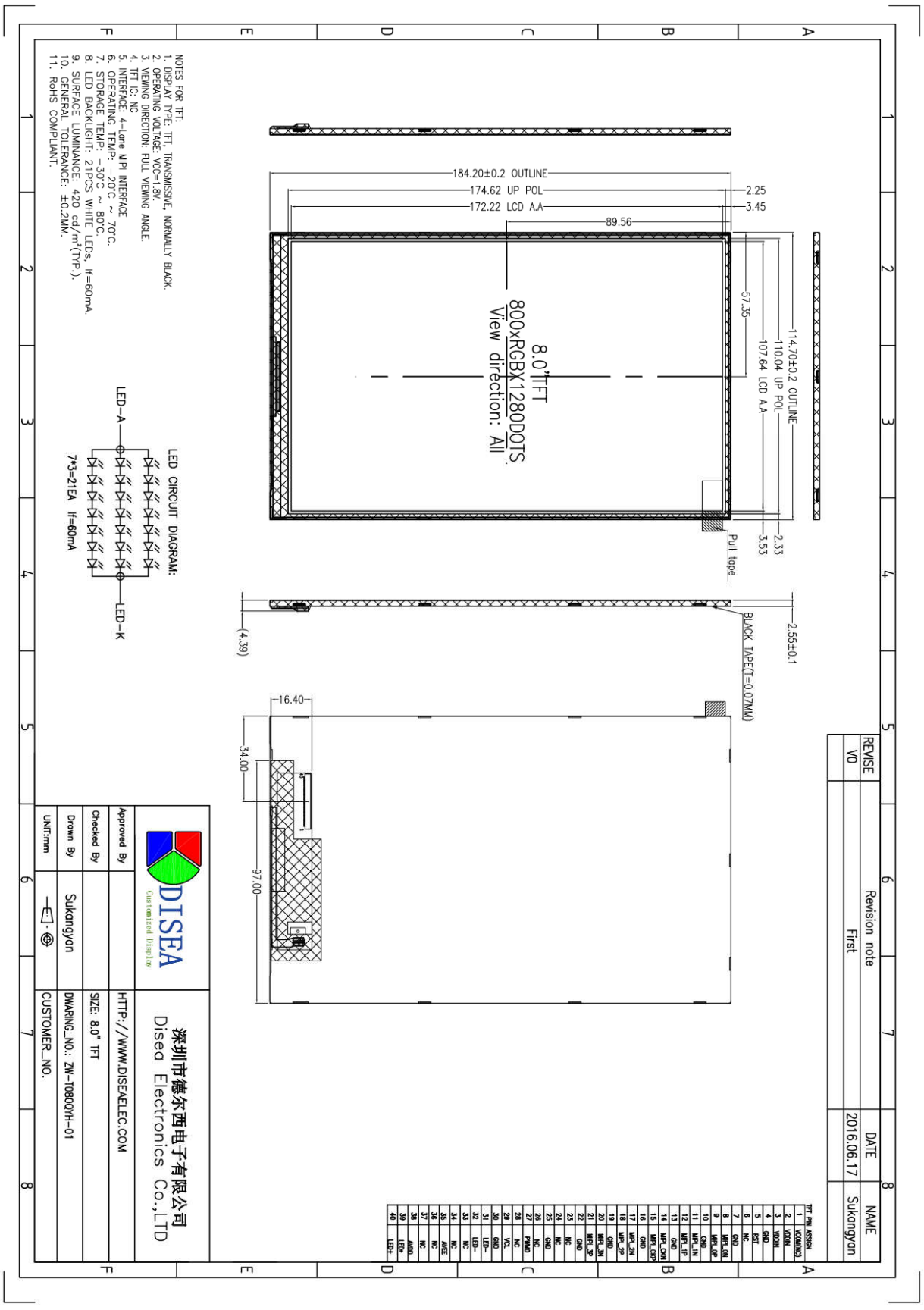
Date	Rev.No	Page	Revision Items	Prepared
2016-07-01	V0		The first release	ZHP
2017-09-26	V1		Update drawing	Stone
2018-08-01	V2		Update the format	mma

3. General Specifications

ZW-T080QYH-01 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The 8.0″ display area contains 800 x1280 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	TFT/Transmissive/Normally White	-	
Display color	16.7M		
Viewing Direction	Full viewing angle	O'Clock	
Operating temperature	-10~+50	℃	
Storage temperature	-20~+60	℃	
Module size	114.7x184.2x2.55	mm	
Active Area(W×H)	107.64X172.22	mm	
Number of Dots	800×1280	dots	
TFT Controller	N/A	-	
Power Supply Voltage	1.8	V	
Backlight	21LEDs (white)	pcs	
Weight	---	g	
Interface	4Lanes-MIPI	-	

4.Outline.Drawing



5. Absolute Maximum Ratings(Ta=25℃)

5.1 Electrical Absolute Maximum Ratings.(Vss=0V ,Ta=25℃)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDDIN	-0.3	5.5	V	1，2
	AVDD	-0.3	6.6		
	AVEE	+0.3	-6.6	V	

Notes:

1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.

5.2 Environmental Absolute Maximum Ratings.

Item	Storage		Operating		Note
	MIN.	MAX.	MIN.	MAX.	
Ambient Temperature	-20℃	60℃	-10℃	50℃	1,2
Humidity	-	-	-	-	3

1. The response time will become lower when operated at low temperature.

2. Background color changes slightly depending on ambient temperature.

The phenomenon is reversible.

3. Ta<=40 ℃:85%RH MAX.

Ta>=40 ℃:Absolute humidity must be lower than the humidity of 85%RH at 40 ℃.

6. Electrical Specifications and Instruction Code

6.1 Electrical characteristics(Vss=0V ,Ta=25℃)

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Power supply		VDDIN	Ta=25℃	1.7	1.8	1.9	V	
		AVDD	Ta=25℃	5.2	5.8	6.0	V	
		AVEE	Ta=25℃	-6.0	-5.8	-5.2	V	
Input voltage	'H'	V_{IH}	-	0.7V_{CC}	-	V_{CC}	V	
	'L'	V_{IL}	-	0	-	0.3V_{CC}	V	
Current Consumption		I_{CC1}	Normal mode	-	-	-	mA	
		I_{CC2}	Sleep mode	-	-	-	mA	

6.2 LED backlight specification(VSS=0V ,Ta=25℃)

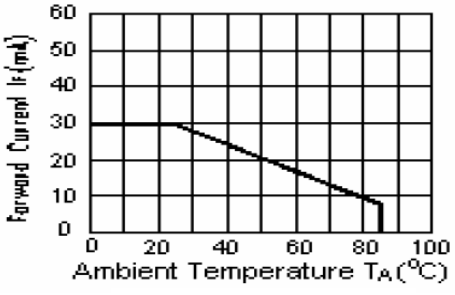
Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply voltage	V_f	If=60mA	19	21	23	V	
Uniformity	∆ Bp	If=60mA	75	-	-	%	
LED life time	–	If=60mA	20k	30k	Hours		

Note:

1: VLED=VLED(+)-VLED(-).

2:The current of LED is 20mA.

A LED drive in constant current mode is recommended.



ILED VS TEMP

6.3 Interface signals

Pin No.	Symbol	I/O	Function
1	VCOM	P	Common Voltage(-1.756 ± 0.3 V)
2-3	VDDIN	P	A power supply for the analog power.
4	GND	P	Ground.
5	RST	I	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied
6	NC	-	No connection
7	GND	P	Ground.
8	MIPI-0N	I	MIPI-DSI Data differential signal input pins. (Data
9	MIPI-0P	I	MIPI-DSI Data differential signal input pins. (Data
10	GND	P	Ground.
11	MIPI-1N	I	MIPI-DSI Data differential signal input pins. (Data
12	MIPI-1P	I	MIPI-DSI Data differential signal input pins. (Data
13	GND	P	Ground.
14	MIPI-CLKN	I	MIPI-DSI CLOCK differential signal input pins.
15	MIPI-CLKP	I	MIPI-DSI CLOCK differential signal input pins.
16	GND	P	Ground.
17	MIPI-2N	I	MIPI-DSI Data differential signal input pins. (Data
18	MIPI-2P	I	MIPI-DSI Data differential signal input pins. (Data
19	GND	P	Ground.
20	MIPI-3N	I	MIPI-DSI Data differential signal input pins. (Data
21	MIPI-3P	I	MIPI-DSI Data differential signal input pins. (Data
22	GND	P	Ground.
23-24	NC	-	No connection
25	GND	P	Ground.
26	NC	-	No connection
27	PWM0	I	CABC PWM signal output.
28	NC	-	No connection
29	VCL	P	Output voltage pin,use it to generate common voltage by a VR circuit (output voltage -2.5V)
30	GND	P	Ground.
31-32	LED-	P	LED back light(Cathode)
35	AVEE	P	Analog supply negative voltage
36-37	NC	-	No connection
38	AVDD	P	Analog supply positive voltage
39-40	LED+	P	LED back light(Anode)

6.4 MIPI signal Timing Characteristics

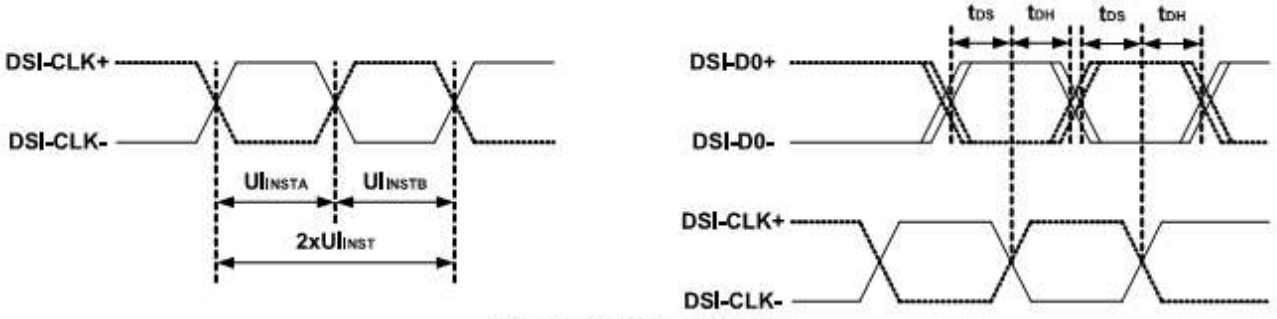
6.4.1 High Speed Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

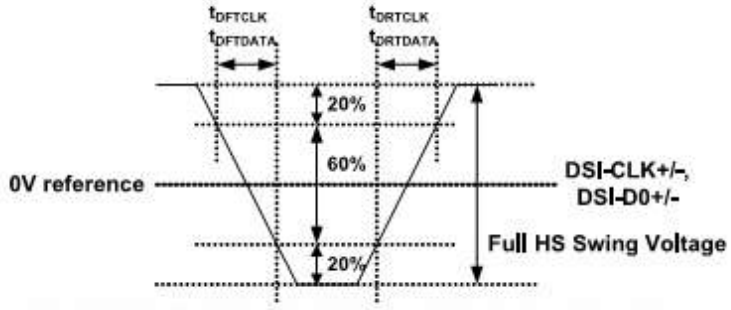
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



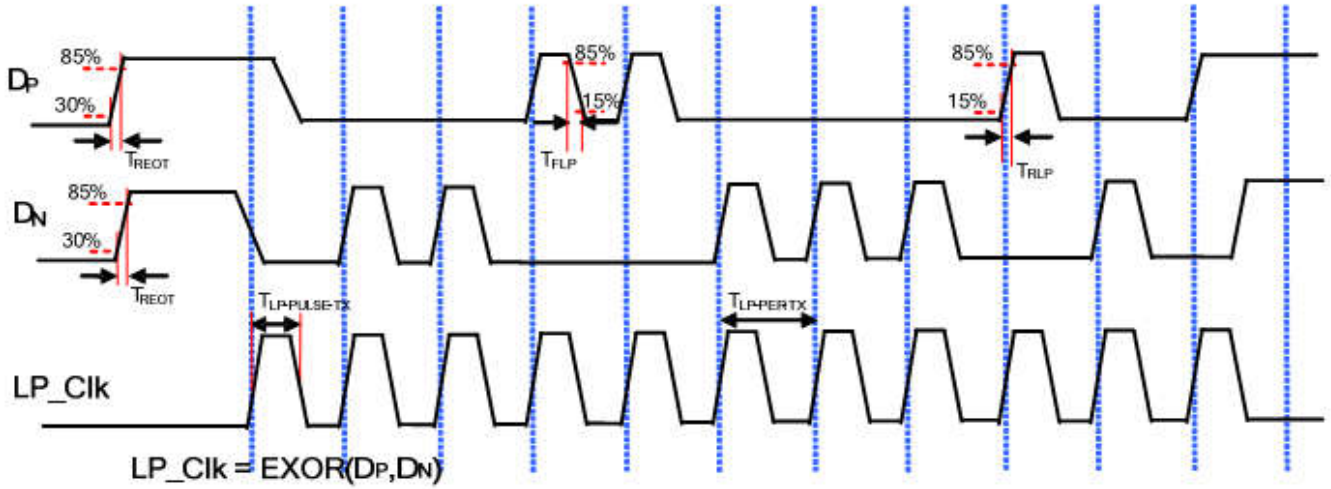
DSI clock channel timing



Rising and fall time on clock and data channel

6.4.2 LP Transmission

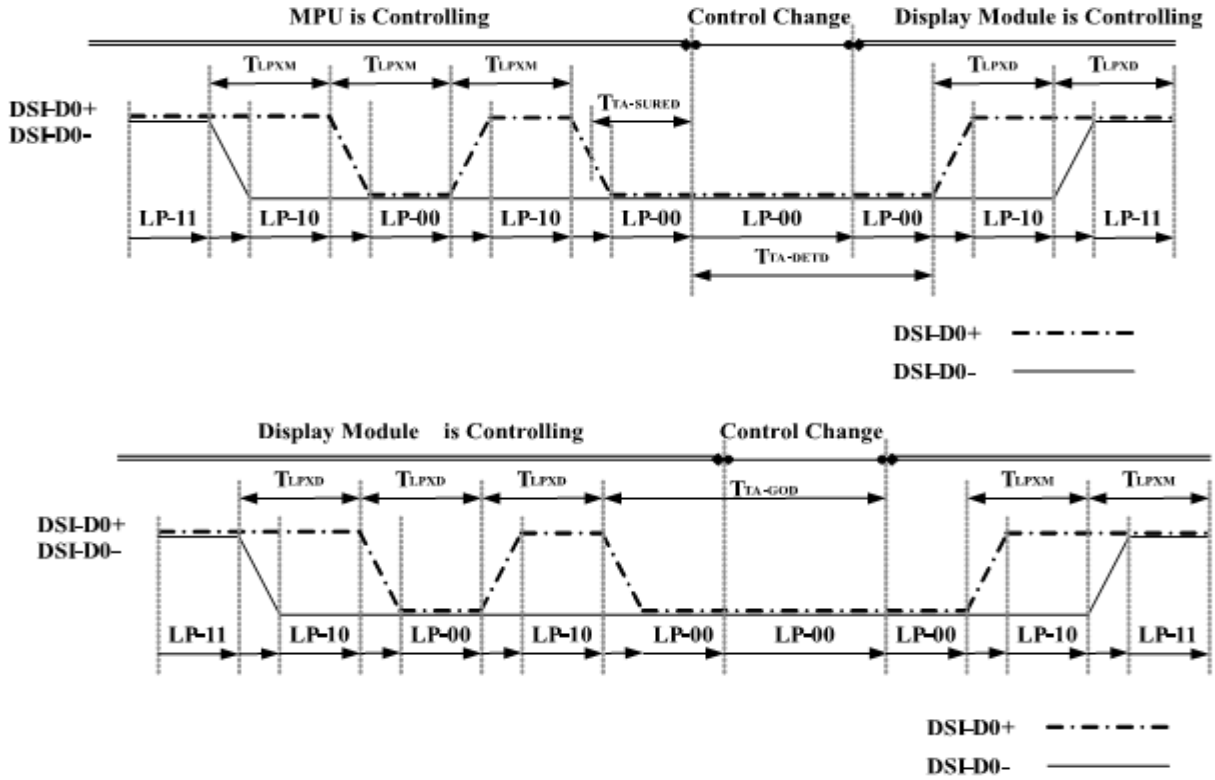
Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP-PULSE-TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP-PRE-TX}$	100	130	-	ns	



6.4.3 Low Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+ /-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU (Display Module	50	-	75	ns	Input
DSI-D0+ /-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (MPU	50	-	75	ns	Output
DSI-D0+ /-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2xTLPXD	ns	Output
DSI-D0+ /-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD	-	-	ns	Input
DSI-D0+ /-	TTA-GOD	Time to drive LP-00 after turnaround request - MPU	4xTLPXD	-	-	ns	Output

Bus Turnaround (BAT) from MPU to display module Timing



Bus Turnaround (BAT) from display module to MPU Timing

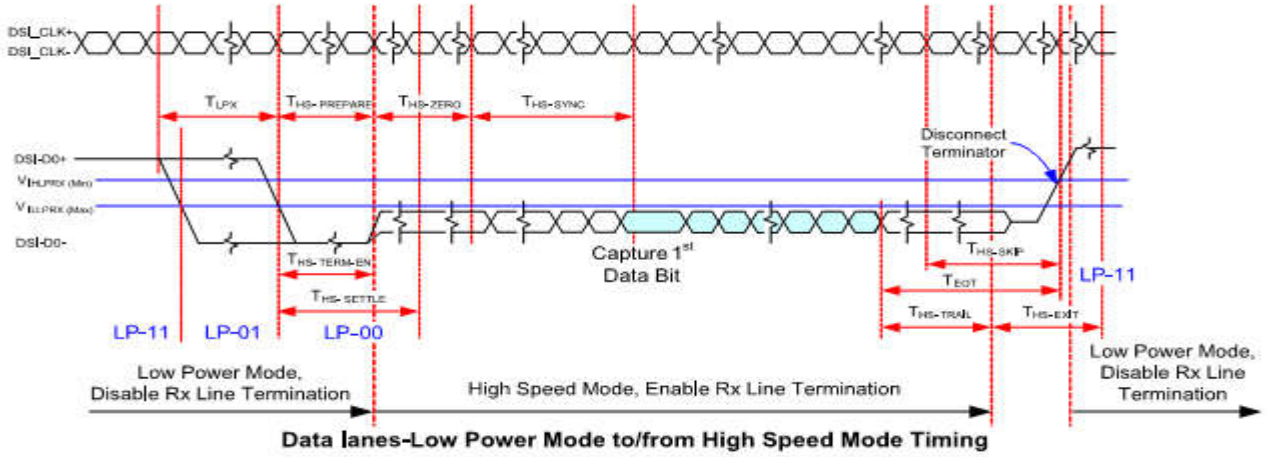
6.4.4 DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to	60+52xUI	-	-	ns	Input

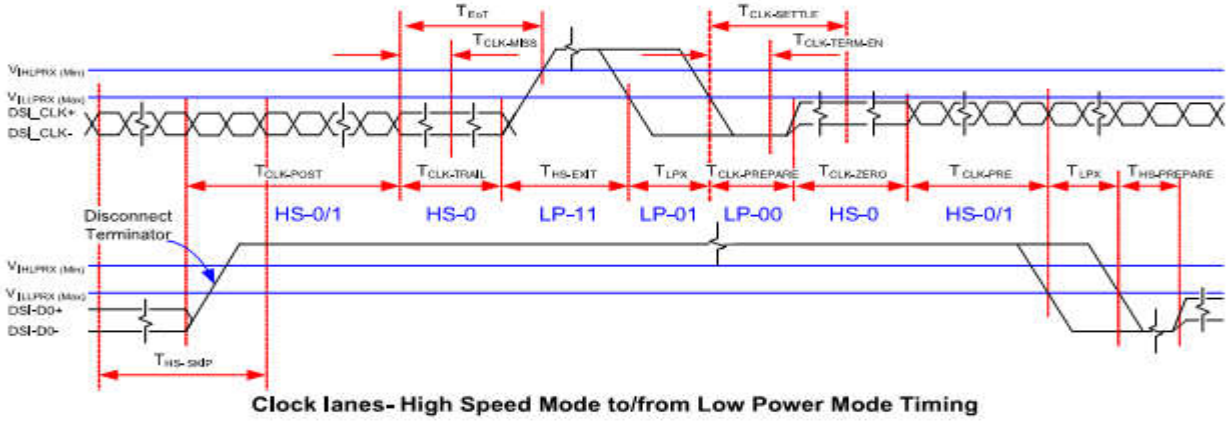
		LP mode					
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

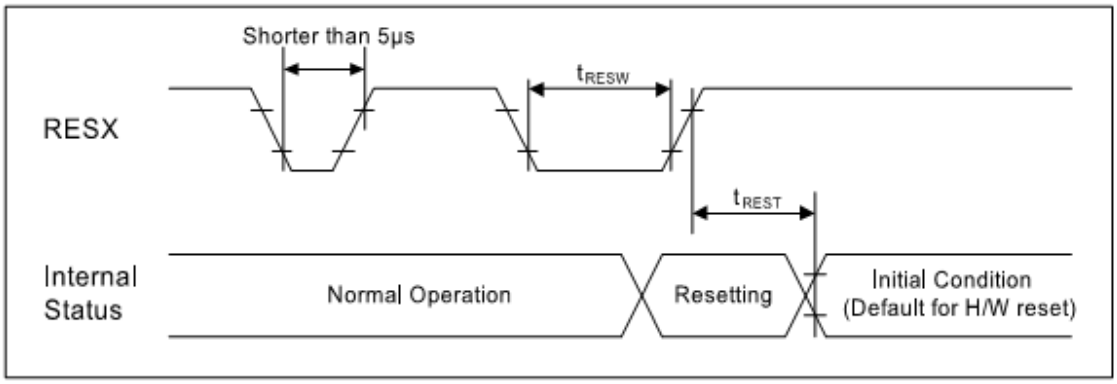


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

6.4.5 Reset Input Timing



Reset input timing
(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

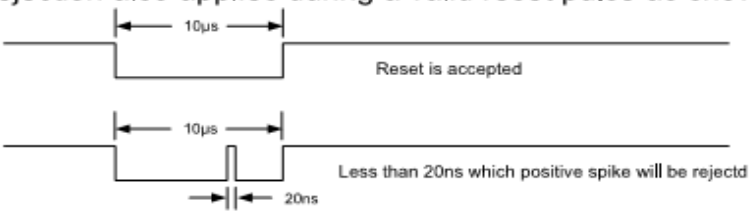
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7. Optical Characteristics

Item	Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Brightness	Bp		θ=0° Φ=0°	350	420	-	Cd/m²	1
Uniformity	⊿Bp			75	-	-	%	1,2
Viewing Angle	3:00		Cr≥10	70	80	-	Deg	3
	6:00			70	80	-		
	9:00			70	80	-		
	12:00			70	80	-		
Contrast Ratio	Cr		θ=0° Φ=0°	600	800	-	-	4
Response Time	T_r			-	25		ms	5
	T_f			-	25		ms	
Color of CIE Coordinate	W	x	θ=0° Φ=0°	-0.05	0.31	+0.05	-	1,6
		y			0.33		-	
	R	x			-		-	
		y			-		-	
	G	x			-		-	
		y			-		-	
	B	x			-		-	
		y			-		-	
NTSC Ratio	S			50	60	-	%	

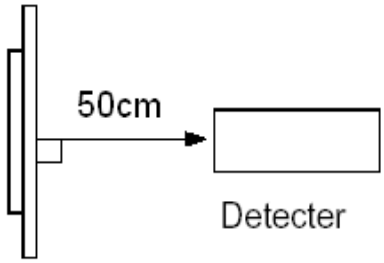
Note：The parameter is slightly changed by temperature, driving voltage and materiel

*Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipm*ent BM-7 (Φ5mm)

Measuring condition:

- *Measuring surroundings: Dark room.*
- *Measuring temperature: Ta=25 ℃.*
- *Adjust operating voltage to get optimum contrast at the center of the display.*

Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

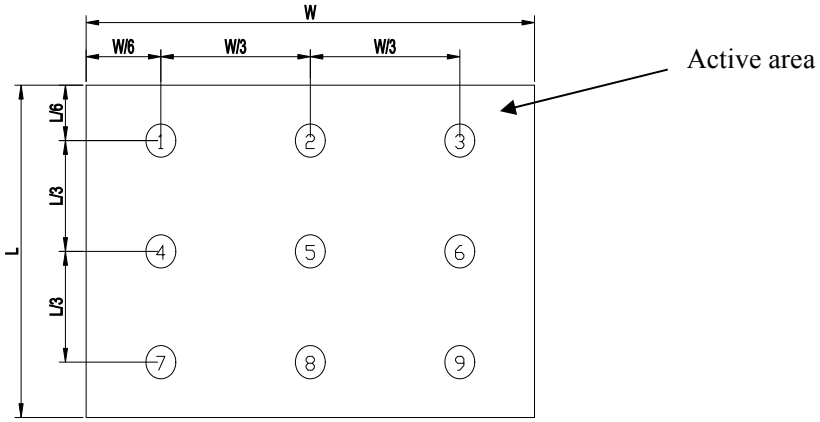


Note 2: The luminance uniformity is calculated by using following formula.

⊿Bp = Bp (Min.) / Bp (Max.)×100 (%)

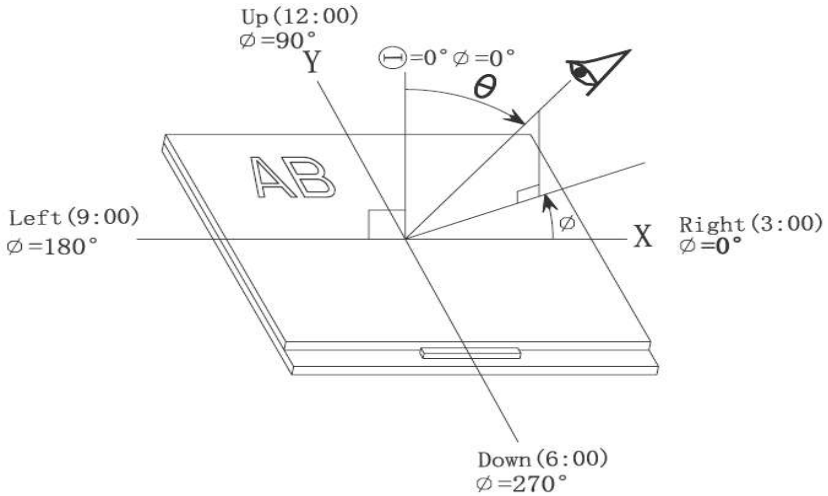
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

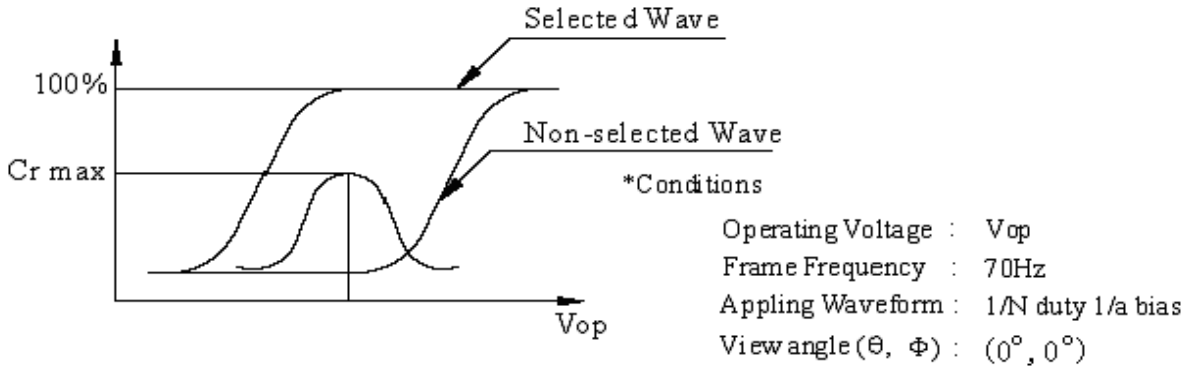


Note 3: The definition of viewing angle:

Refer to the graph below marked by ϑ and Φ



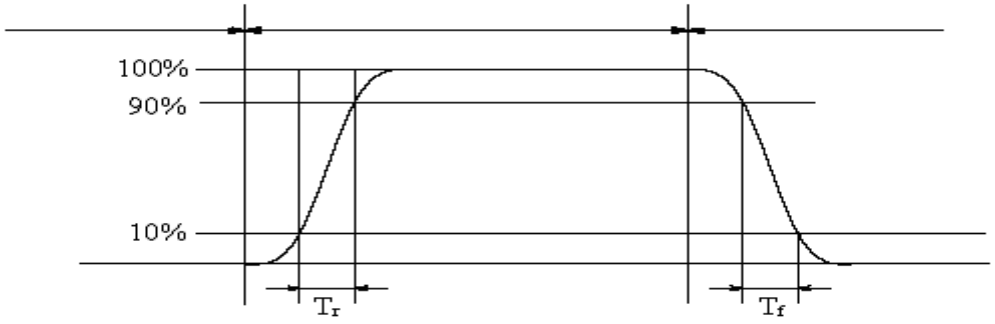
Note 4: Definition of contrast ratio.(Test LCD using DMS501)



$$Contrast\ ratio(Cr) = \frac{Brightness\ of\ selected\ dots}{Brightness\ of\ non-selected\ dots}$$

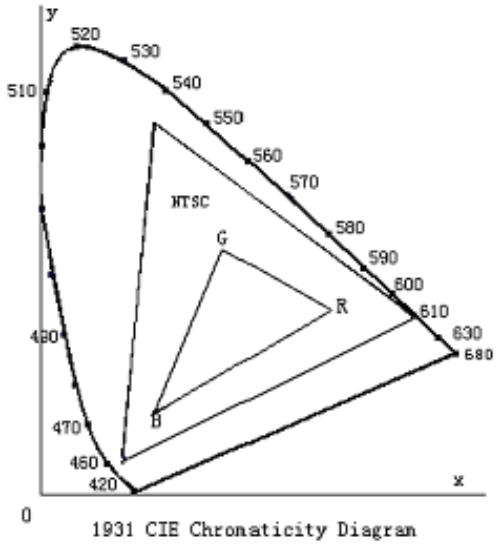
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "black" to "white"(falling time) and from "white" to "black"(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes.Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.



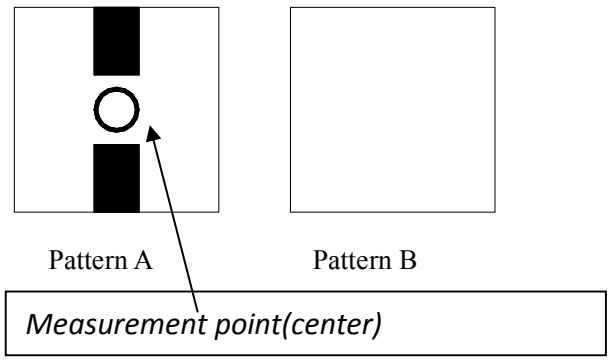
1931 CIE Chromaticity Diagram

Color gamut:

$$\mathbf{S = \frac{area\ of\ RGB\ triangle}{area\ of\ NTSC\ triangle} \times 100\%}$$

Note 7: Definition of cross talk.

*Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness*100*



Electric volume value=3F+/-3Hex

8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	60℃±2℃ 96H Restore 2H at 25℃ Power off	1. After testing, cosmetic and electrical defects should not happen. 2. Total current consumption should not be more than twice of initial value.
2	Low Temperature Storage	-20℃±2℃ 96H Restore 2H at 25℃ Power off	
3	High Temperature Operation	50℃±2℃ 96H Restore 2H at 25℃ Power on	
4	Low Temperature Operation	-10℃±2℃ 96H Restore 4H at 25℃ Power on	
5	High Temperature/Humidity Operation	40℃±2℃ 90%RH 96H Power on	
6	Temperature Cycle	-20℃←→60℃ 30min 5min 30min after 5 cycle, Restore 2H at 25℃ Power off	
7	Vibration Test	10Hz~150Hz, 100m/s^2, 120min	Not allowed cosmetic and electrical defects.
8	Shock Test	Half- sine wave,300m/s^2,11ms	

Note: Operation: Supply 1.8V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

9. Precautions for Use of LCD Modules

9.1 Handling Precautions

9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol — Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

9.1.6 Do not attempt to disassemble the LCD Module.

9.1.7 If the logic circuit power is off, do not apply the input signals.

9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

9.2 Storage precautions

9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

9.3 ***The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.***

END

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