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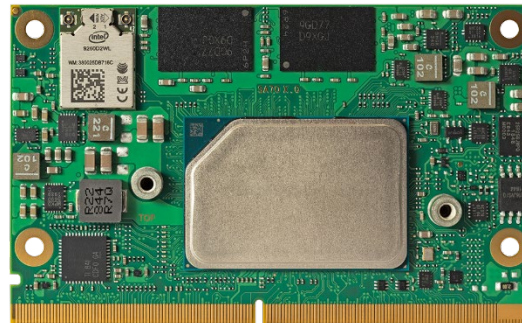


Manual

Congatec

conga-SA7

SMARC™ 2.1 Computer-on-Module with Intel® Elkhart Lake Processor



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SMARC[®] conga-SA7

SMARC 2.1 module based on Intel[®] Atom[®], Pentium[®] and Celeron[®] Elkhart Lake SoC

User's Guide

Revision 1.00

Revision History

| Revision | Date (yyyy-mm-dd) | Author | Changes |
|----------|-------------------|--------|---|
| 0.1 | 2021-04-22 | AEM | <ul style="list-style-type: none">• Preliminary release |
| 1.00 | 2021-09-28 | AEM | <ul style="list-style-type: none">• Added Software License Information• Removed product variant with part number 050122 from table 1 "Commercial Variants" and table 5 "Power Consumption Values"• Corrected the Operating System used for measuring power consumption• Updated table 5 "Power Consumption Values" and table 6 "CMOS Battery Power Consumption"• Added section 6.2 "eMMC"• Updated section 6.6 "congatec Battery Management Interface"• Added section 9 "System Resources"• Official release |

Preface

This user's guide provides information about the components, features, connectors and BIOS Setup menus available on the conga-SA7. It is one of three documents that should be referred to when designing a SMARC® application. The other reference documents that should be used include the following:

SMARC® Design Guide 2.0

SMARC® Specification 2.1

The links to the SMARC® documents can be found on the SGET website at www.sget.org.

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Terminology

| Term | Description |
|-------|---------------------------|
| GB | Gigabyte |
| GHz | Gigahertz |
| kB | Kilobyte |
| MB | Megabyte |
| MT/s | Mega-transfers per second |
| Mbit | Megabit |
| kHz | Kilohertz |
| MHz | Megahertz |
| TDP | Thermal Design Power |
| cBC | congatec Board Controller |
| PCIe | PCI Express |
| SATA | Serial ATA |
| PEG | PCI Express Graphics |
| PCH | Platform Controller Hub |
| eDP | Embedded DisplayPort |
| DDI | Digital Display Interface |
| HDA | High Definition Audio |
| N.C | Not connected |
| N.A | Not available |
| T.B.D | To be determined |

Contents

| | | | | | |
|-------|---|----|---------|---|----|
| 1 | Introduction | 11 | 5.6 | Audio (HDA)..... | 29 |
| 1.1 | SMARC® Concept | 11 | 5.7 | SD Card..... | 30 |
| 1.2 | conga-SA7 Options Information | 11 | 5.8 | UART | 30 |
| 1.2.1 | Options Information..... | 12 | 5.9 | GPIO | 30 |
| 2 | Specifications | 13 | 5.10 | SPI..... | 31 |
| 2.1 | Feature List | 13 | 5.11 | I2C | 31 |
| 2.2 | Supported Operating Systems | 14 | 5.12 | Power Control | 31 |
| 2.3 | Mechanical Dimensions | 14 | 6 | Additional Features..... | 34 |
| 2.4 | Standard Power..... | 15 | 6.1 | Optional Onboard Interfaces..... | 34 |
| 2.4.1 | Supply Voltage..... | 15 | 6.2 | eMMC | 34 |
| 2.4.2 | Electrical Characteristics | 15 | 6.3 | Security Features..... | 34 |
| 2.4.3 | Rise Time | 15 | 6.4 | congatec Board Controller (cBC) | 34 |
| 2.5 | Power Consumption | 16 | 6.4.1 | Board Information | 34 |
| 2.6 | Supply Voltage Battery Power | 17 | 6.4.2 | General Purpose Input/Output..... | 35 |
| 2.7 | Environmental Specifications..... | 18 | 6.4.3 | Fan Control | 35 |
| 3 | Block Diagram..... | 19 | 6.4.4 | Power Loss Control | 35 |
| 4 | Cooling Solutions..... | 20 | 6.4.5 | Watchdog | 35 |
| 4.1 | CSP Dimensions..... | 21 | 6.4.6 | Enhanced Soft-Off State | 36 |
| 4.2 | CSP Dimensions | 22 | 6.5 | OEM BIOS Customization..... | 36 |
| 4.3 | HSP Dimensions..... | 23 | 6.5.1 | OEM Default Settings | 36 |
| 4.4 | HSP Dimensions..... | 24 | 6.5.2 | OEM Boot Logo..... | 36 |
| 5 | Connector Rows..... | 25 | 6.5.3 | OEM POST Logo | 36 |
| 5.1 | PCI Express™ | 25 | 6.5.4 | OEM BIOS Code/Data..... | 37 |
| 5.1.1 | Possible Reference Clock Configuration..... | 25 | 6.5.5 | OEM DXE Driver | 37 |
| 5.2 | Display Interfaces..... | 26 | 6.6 | congatec Battery Management Interface | 37 |
| 5.2.1 | LVDS..... | 27 | 6.7 | API Support (CGOS) | 38 |
| 5.2.2 | HDMI..... | 27 | 6.8 | congatec System Sensors | 38 |
| 5.2.3 | DP ++ | 28 | 6.9 | Suspend to Ram..... | 38 |
| 5.3 | SATA | 28 | 7 | conga Tech Notes | 39 |
| 5.4 | Gigabit Ethernet | 28 | 7.1 | Intel® Elkhart Lake SoC Features..... | 39 |
| 5.5 | USB | 29 | 7.1.1 | Processor Core..... | 39 |
| | | | 7.1.1.1 | Intel® Virtualization Technology | 39 |
| | | | 7.1.1.2 | AHCI | 40 |
| | | | 7.1.1.3 | Thermal Management | 40 |

| | | |
|--------|--|----|
| 7.2 | ACPI Suspend Modes and Resume Events..... | 41 |
| 7.3 | USB Port Mapping | 42 |
| 8 | Signal Descriptions and Pinout Tables..... | 43 |
| 9 | System Resources | 65 |
| 9.1 | I/O Address Assignment..... | 65 |
| 9.2 | PCI Configuration Space Map | 66 |
| 9.3 | I ² C Bus and SMBus | 67 |
| 10 | BIOS Setup Description | 68 |
| 10.1 | Navigating the BIOS Setup Menu | 68 |
| 10.2 | BIOS Versions..... | 68 |
| 10.3 | Updating the BIOS..... | 68 |
| 10.3.1 | Update from External Flash | 69 |
| 10.4 | Supported Flash Devices | 69 |

List of Tables

| | | |
|----------|---|----|
| Table 1 | Commercial Variants | 12 |
| Table 2 | Industrial Variants..... | 12 |
| Table 3 | Feature Summary | 13 |
| Table 4 | Measurement Description..... | 16 |
| Table 5 | Power Consumption Values | 17 |
| Table 6 | CMOS Battery Power Consumption | 17 |
| Table 7 | Cooling Solution Variants..... | 20 |
| Table 8 | PCIe Reference Clock Configuration | 25 |
| Table 9 | Display Combination | 26 |
| Table 10 | Possible USB Port Mapping..... | 29 |
| Table 11 | Wake Events..... | 41 |
| Table 12 | Signal Tables Terminology Descriptions | 43 |
| Table 13 | SMARC Edge Finger Pinout..... | 44 |
| Table 14 | LVDS Signal Description | 49 |
| Table 15 | HDMI Signal Descriptions..... | 52 |
| Table 16 | DisplayPort++ | 53 |
| Table 17 | MIPI CSI-2/-3..... | 53 |
| Table 18 | SDIO Signal Descriptions..... | 54 |
| Table 19 | SPI0 Signal Descriptions | 55 |
| Table 20 | eSPI/SPI1 Signal Descriptions..... | 55 |
| Table 21 | I2S Signal Descriptions | 56 |
| Table 22 | HDA / I2S Signal Descriptions | 56 |
| Table 23 | I2C Signal Descriptions..... | 56 |
| Table 24 | Asynchronous Serial Port Signal Description | 57 |
| Table 25 | USB Pinout Description..... | 57 |
| Table 26 | PCIe Signal Description | 58 |
| Table 27 | SERDES Signal Description..... | 59 |
| Table 28 | SATA Signal Description | 59 |
| Table 29 | Gigabit Ethernet Signal Description | 60 |
| Table 30 | Watchdog Signal Description | 60 |
| Table 31 | GPIO Signal Description | 61 |
| Table 32 | Management Pins Signal Description | 62 |
| Table 33 | Boot Select Signal Description | 63 |
| Table 34 | Power and GND Signal Descriptions | 64 |
| Table 35 | I/O Address Assignment..... | 65 |
| Table 36 | Bus Accessibility..... | 67 |

1 Introduction

1.1 SMARC® Concept

The Standardization Group for Embedded Technologies e.V (SGET) defined the SMARC standard for small form factor computer modules that target applications with ultra low power, low cost and high performance. The SMARC connector and interfaces are optimized for high-speed communication, and are suitable for ARM SoCs and low power x86 SoCs.

The SMARC standard bridges the gap between the COM Express standard and the Qseven standard by offering most of the interfaces defined in the COM Express specification at a lower power. With a footprint of 82 mm x 50 mm or 82 mm x 80 mm, the SMARC standard promotes the design of highly integrated, energy efficient systems.

Due to its small size and lower power demands, PC appliance designers can design low cost devices as well as explore a huge variety of product development options—from compact space-saving designs to fully functional systems. This solution allows scalability, product diversification and faster time to market.

1.2 conga-SA7 Options Information

The conga-SA7 design is based on the SMARC 2.1 Specification. The conga-SA7 features the Intel® Atom®, Pentium® and Celeron® Elkhart Lake SoCs. With maximum 12 W TDP, the conga-SA7 offers Ultra Low Power boards with high computing performance and outstanding graphics. Additionally, the conga-SA7 supports quad channel LPDDR4x memory with up to 16 GB capacity and data rates up to 4267 MT/s, multiple I/O interfaces, up to three independent displays and various congatec embedded features.

By offering most of the functional requirement for any SMARC application, the conga-SA7 provides manufacturers and developers with a platform to jump-start the development of systems and applications based on SMARC specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.2.1 Options Information

The conga-SA7 is available in eight variants (five commercial and three industrial). The table below shows the different configurations available.

Table 1 Commercial Variants

| Part-No | 050100 | 050101 | 050102 | 050120 | 050121 |
|--------------------------|---|---|---|---|---|
| Processor | Intel® Atom® x6425E 2.0 GHz, Quad Core | Intel® Atom® x6413E 1.5 GHz, Quad Core | Intel® Atom® x6211E 1.3 GHz, Dual Core | Intel® Pentium® J6426 2.0 GHz, Quad Core | Intel® Celeron® J6413 1.8 GHz, Quad Core |
| Burst Freq. | 3.0 GHz | 3.0 GHz | 3.0 GHz | 3.0 GHz | 3.0 GHz |
| L2 Cache | 1.5 MB | 1.5 MB | 1.5 MB | 1.5 MB | 1.5 MB |
| Graphics Engine | Intel® UHD Graphics | Intel® UHD Graphics | Intel® UHD Graphics | Intel® UHD Graphics | Intel® UHD Graphics |
| GFX Base/Burst Freq. | 500 / 750 MHz | 500 / 750 MHz | 350 / 750 MHz | 400 / 850 MHz | 400 / 800 MHz |
| Onboard Memory (LPDDR4x) | 16 GB, 3200 MT/s quad channel | 8 GB, 3200 MT/s quad channel | 4 GB, 3200 MT/s quad channel | 16 GB, 3200 MT/s quad channel | 8 GB, 3733 MT/s quad channel |
| eMMC | 64 GB | 32 GB | 32 GB | 64 GB | 32 GB |
| Wifi/BT Module | N.A | N.A | N.A | N.A | N.A |
| TPM (Discrete) | Infineon SLB9670 | Infineon SLB9670 | Infineon SLB9670 | Infineon SLB9670 | Infineon SLB9670 |
| SD Card | 1x 4-bit | 1x 4-bit | 1x 4-bit | 1x 4-bit | 1x 4-bit |
| Max. TDP | 12 W | 9 W | 6 W | 10 W | 10 W |

Table 2 Industrial Variants

| Part-No | 050110 | 050111 | 050112 |
|--------------------------|--|--|--|
| Processor | Intel® Atom® x6425RE 1.9 GHz, Quad Core | Intel® Atom® x6414RE 1.5 GHz, Quad Core | Intel® Atom® x6212RE 1.2 GHz, Dual Core |
| Burst Freq. | N.A | N.A | N.A |
| L2 Cache | 1.5 MB | 1.5 MB | 1.5 MB |
| Graphics Engine | Intel® UHD Graphics | Intel® UHD Graphics | Intel® UHD Graphics |
| GFX Base/Burst Freq. | 400 MHz/ N.A | 400 MHz/ N.A | 350 MHz/ N.A |
| Onboard Memory (LPDDR4x) | 8 GB, 4267 MT/s quad channel | 4 GB, 3200 MT/s quad channel | 4 GB, 3200 MT/s quad channel |
| eMMC | 32 GB | 32 GB | 32 GB |
| Wifi/BT Module | N.A | N.A | N.A |
| TPM (Discrete) | Infineon SLB9670 | Infineon SLB9670 | Infineon SLB9670 |
| SD Card | 1x 4-bit | 1x 4-bit | 1x 4-bit |
| Max. TDP | 12 W | 9 W | 6 W |

2 Specifications

2.1 Feature List

Table 3 Feature Summary

| | | |
|---------------------------|---|---|
| Form Factor | SMARC® form factor specification, revision 2.1 (82 mm x 50 mm) | |
| SoC | Intel® Atom®, Pentium® and Celeron SoCs | |
| Memory | Onboard non-ECC LPDDR4x memory. Supports <ul style="list-style-type: none"> - data rates up to 4267 MT/s - up to 16 GB capacity - in-band ECC (out of band ECC is not supported) | |
| Chipset | Integrated in the SoC | |
| Audio | Intel High Definition Audio | |
| Ethernet | 2x Gigabit Ethernet via TI DP83867CS/IS Ethernet PHY (with TSN support) | |
| Graphics Options | Intel® UHD (Gen 11). Supports: <ul style="list-style-type: none"> - API (DirectX 12.1, OpenGL 4.5, OpenCL 1.2, OpenGL ES 3.1, Vulkan 1.0) - Intel® QuickSync & Clear Video Technology HD (hardware accelerated video decode/encode/processing/transcode) - up to 3 independent displays (must be two DDI's and one LVDS/eDP/DSI) | |
| | 1x LVDS (dual channel) 1x DP++ 1x HDMI 2.0b (native) | Optional Interface (assembly option): <ul style="list-style-type: none"> - 1x eDP 1.3¹ or 1x MIPI-DSI (x4 lane)¹ - 1x DP++ (DDI1)² |
| Peripheral Interfaces | 1x SATA® 6 Gb/s Up to 4x PCIe® Gen3 ports 6x USB 2.0 (1x USB dual role) 2x USB 3.1 Gen 2 (1x USB dual role) 4x UART (two with handshake signals) 1x SD/SDIO | 2x I ² C 1x HDA 2x SPI (1x eSPI and 1x SPI) Optional Interface (assembly option): <ul style="list-style-type: none"> - M.2 1216 Wi-Fi/BT module³ |
| Mass Storage | eMMC 5.1 onboard flash | |
| BIOS | AMI Aptio® V UEFI 2.x firmware 32 MB serial SPI with congatec Embedded BIOS features | |
| congatec Board Controller | Multi-stage watchdog, non-volatile user data storage, manufacturing and board information, board statistics, hardware monitoring, fan control, I2C bus, Power loss control | |
| Power Mgmt. | ACPI 5.0 compliant with battery support S5e mode (see section 6.3.6 "Enhanced Soft-Off State") Also supports Suspend to RAM (S3) Configurable TDP | |
| Security | Discrete SPI TPM 2.0 (Infineon SLB9670VQ2.0) | |



Note

1. No LVDS support with this option
2. No HDMI support with this option
3. Not available by default

2.2 Supported Operating Systems

The conga-SA7 supports the following operating systems:

- Microsoft® Windows® 10 IoT Enterprise (64-bit)
- Linux Ubuntu (64-bit)
- Android 10 (64-bit)
- Yocto (64-bit)
- RTS Hypervisor



Note

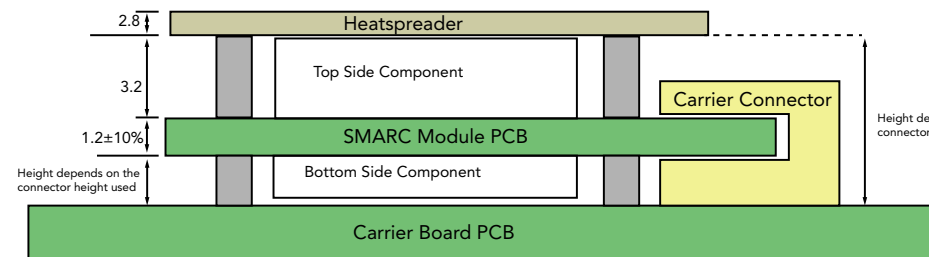
We do not offer installation support for systems with less than 20 GB storage space.

2.3 Mechanical Dimensions

The conga-SA7 has the following dimensions:

- length of 82 mm
- width of 50 mm

The overall height (module, heatspreader and stack) is shown below:

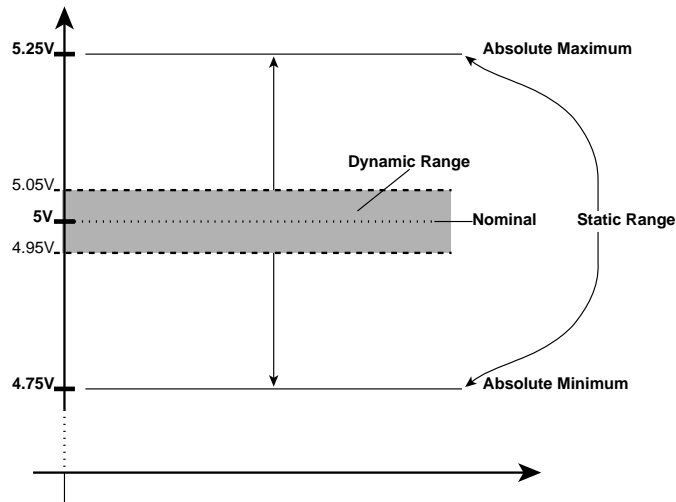


All dimensions are in millimeters

2.4 Standard Power

2.4.1 Supply Voltage

The conga-SA7 provides a supply voltage range of 4.75 V – 5.25 V.



2.4.2 Electrical Characteristics

| Characteristics | | | Min. | Typ. | Max. | Units | Comment |
|-----------------|---------|------|------|------|------|------------------|---------|
| 5V | Voltage | ± 5% | 4.75 | 5.00 | 5.25 | V _{dc} | |
| | Ripple | | - | - | ± 50 | mV _{pp} | 0–20MHz |
| | Current | | | | | | |

2.4.3 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-SA7 COM
- conga-SEVA carrier board
- conga-SA7 cooling solution
- Microsoft® Windows® 10 IoT Enterprise

Table 4 Measurement Description

The power consumption values were recorded during the following system states:

| System State | Description | Comment |
|-------------------|---|--|
| S0: Minimum value | Lowest frequency mode (LFM) with minimum core voltage during desktop idle | |
| S0: Maximum value | Highest frequency mode (HFM/Turbo Boost) | The CPU was stressed to its maximum frequency |
| S0: Peak value | Highest power spike during the measurement of "S0: Maximum value". This state shows the peak value over a short period of time (worst case power consumption value) | Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios |
| S3 | COM is powered by VCC_5V, while in Suspend to RAM state | |
| S5 | COM is powered by VCC_5V, while in Soft-Off state | |
| S5e | COM is powered by VCC_5V, while in enhanced Soft-Off state | |



The peripherals did not influence the measured values because they were powered externally.

Table 5 Power Consumption Values

The table below provides additional information about the conga-SA7 power consumption. The values were recorded at various operating mode.

| Part No. | Memory Size | H.W Rev. | BIOS Rev. | OS (64 bit) | CPU | | | Current (A) | | | | | |
|----------|-------------|----------|-----------|-------------|-----------------------|-------|-------------------|-------------|---------|----------|------|------|-------|
| | | | | | Variant | Cores | Freq. /Max. Turbo | S0: Min | S0: Max | S0: Peak | S3 | S5 | S5e |
| 050100 | 16 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6425E | 4 | 2.0 / 3.0 GHz | 1.28 | 4.50 | 6.02 | 0.36 | 0.34 | 0.002 |
| 050101 | 8 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6413E | 4 | 1.5 / 3.0 GHz | 1.28 | 3.70 | 5.60 | 0.36 | 0.34 | 0.002 |
| 050102 | 4 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6211E | 2 | 1.3 / 3.0 GHz | 1.26 | 2.76 | 4.58 | 0.38 | 0.34 | 0.002 |
| 050110 | 8 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6425RE | 4 | 1.9 GHz/ N.A | 1.28 | 2.98 | 3.22 | 0.38 | 0.34 | 0.002 |
| 050111 | 4 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6414RE | 4 | 1.5 GHz/ N.A | 1.18 | 2.48 | 2.88 | 0.36 | 0.34 | 0.002 |
| 050112 | 4 GB | B.3 | SA70R007 | Windows 10 | Intel® Atom® x6212RE | 2 | 1.2 GHz/ N.A | 1.08 | 1.80 | 2.22 | 0.36 | 0.34 | 0.002 |
| 050120 | 16 GB | B.3 | SA70R007 | Windows 10 | Intel® Pentium® J6426 | 4 | 2.0 / 3.0 GHz | 1.30 | 4.18 | 5.98 | 0.36 | 0.34 | 0.002 |
| 050121 | 8 GB | B.3 | SA70R007 | Windows 10 | Intel® Celeron® J6413 | 4 | 1.8 / 3.0 GHz | 1.42 | 4.06 | 5.82 | 0.36 | 0.34 | 0.002 |



With fast input voltage rise time, the inrush current may exceed the measured peak current.

2.6 Supply Voltage Battery Power

Table 6 CMOS Battery Power Consumption

| RTC @ | Voltage | Current |
|-------|---------|---------|
| -10°C | 3V DC | 1.78 µA |
| 20°C | 3V DC | 1.92 µA |
| 70°C | 3V DC | 2.62 µA |



1. Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.
2. Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).
3. Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf on congatec GmbH website at www.congatec.com/support/application-notes.
4. We recommend to always have a CMOS battery present when operating the conga-SA7

2.7 Environmental Specifications

| | | |
|-----------------------------------|-------------------------|------------------------|
| Temperature (commercial variants) | Operation: 0° to 60°C | Storage: -20° to +80°C |
| Temperature (industrial variants) | Operation: -40° to 85°C | Storage: -40° to +85°C |
| Humidity | Operation: 10% to 90% | Storage: 5% to 95% |

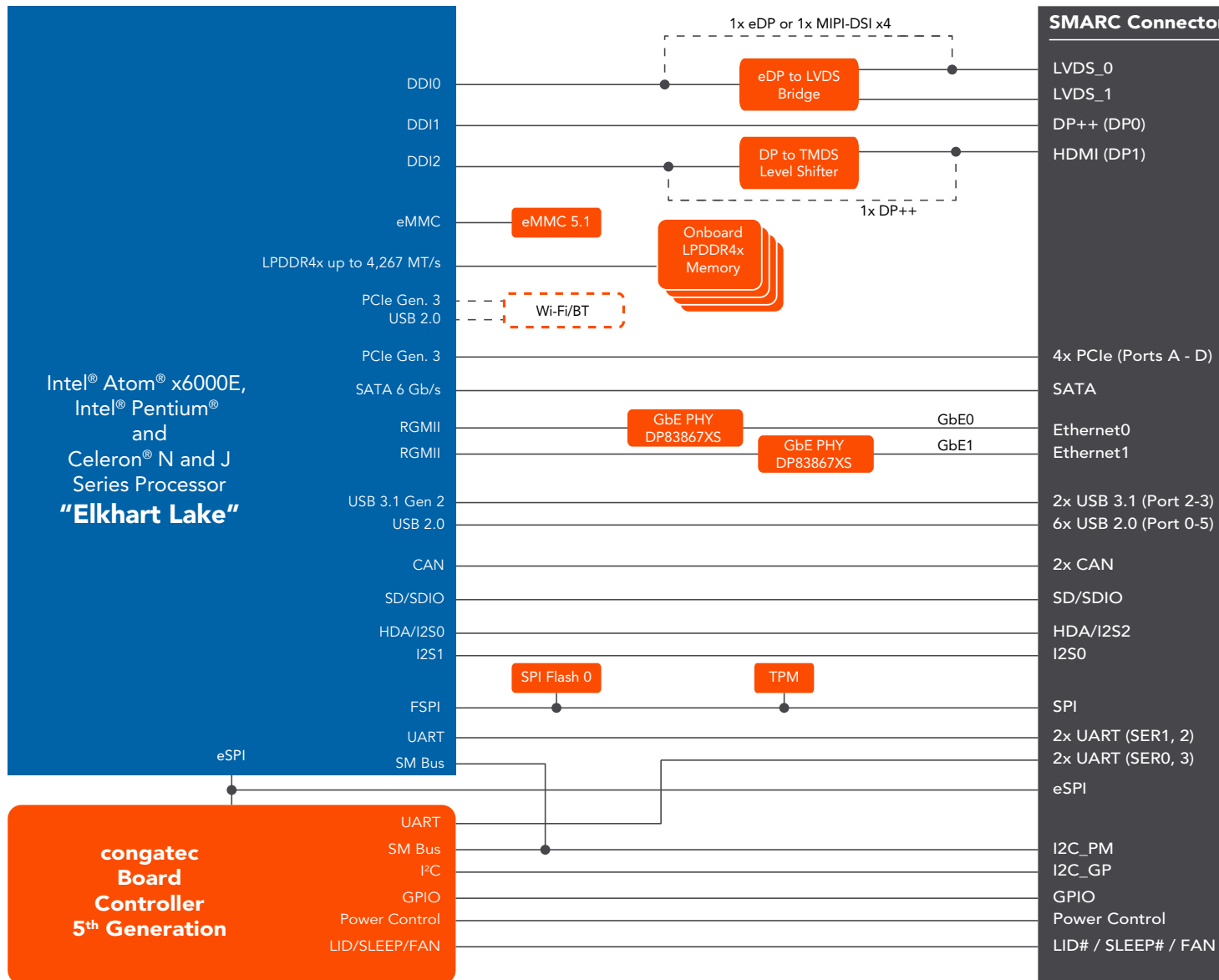


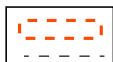
Caution

The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.

Humidity specifications are for non-condensing conditions.

3 Block Diagram



 = Optional - Not available by default

4 Cooling Solutions

congatec GmbH offers the following cooling solutions for the conga-SA7 variants. The dimensions of the cooling solutions are shown in the sub-sections. All measurements are in millimeters.

Table 7 Cooling Solution Variants

| | Cooling Solution | Part No | Description |
|---|------------------|---------|---|
| 1 | CSP | 050150 | Passive cooling with 2.7 mm bore-hole standoffs for lidded CPU variants (industrial variants) |
| | | 050153 | Passive cooling with 2.7 mm bore-hole standoffs for bare-die CPU variants (commercial variants) |
| 2 | HSP | 050151 | Heatspreader with 2.7 mm bore-hole standoffs for lidded CPU variants (industrial variants) |
| | | 050152 | Heatspreader with 2.7 mm bore-hole standoffs for bare-die CPU variants (commercial variants) |



Note

1. We recommend a maximum torque of 0.4 Nm for carrier board mounting screws and 0.5 Nm for module mounting screws.
2. The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.

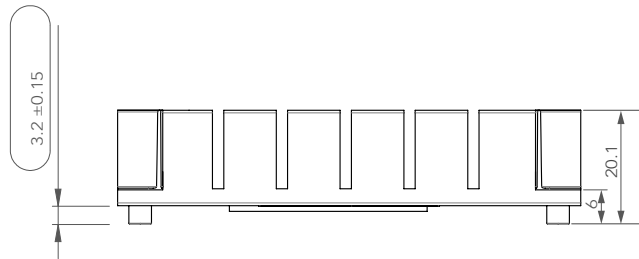
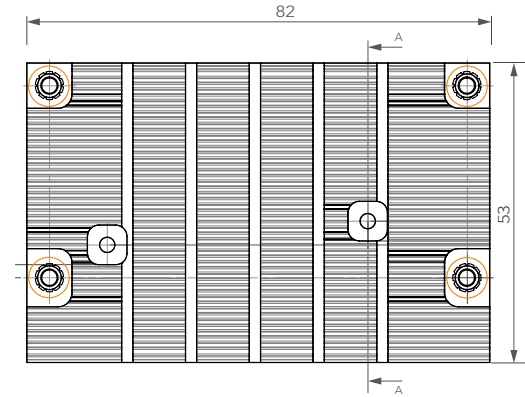
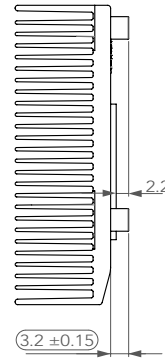
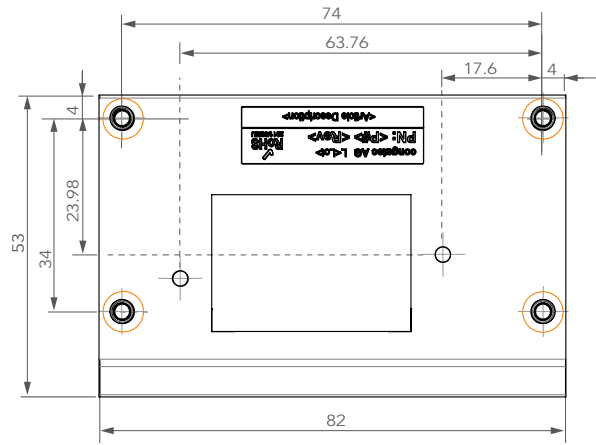



Caution

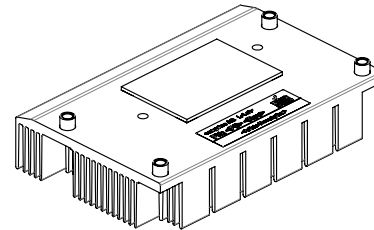
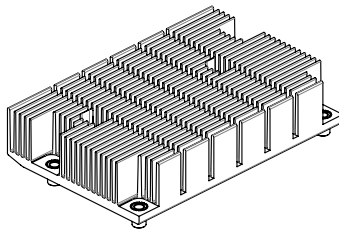
1. The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.
2. For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.
3. For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.
4. Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.

4.1 CSP Dimensions

Lidded Variants (Industrial)

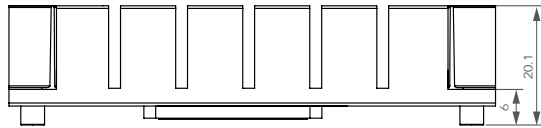
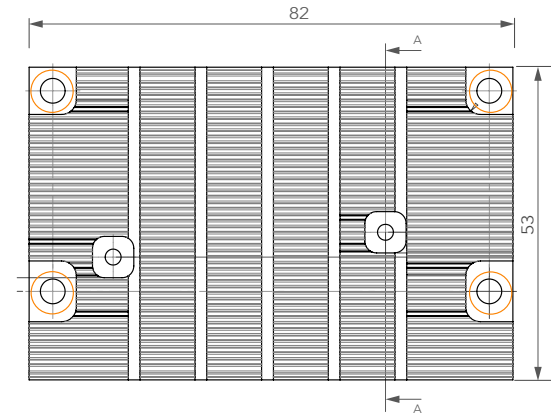
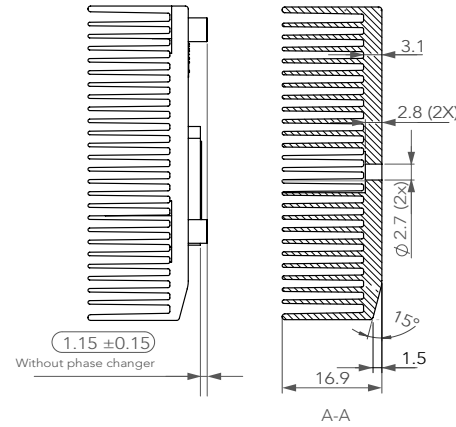
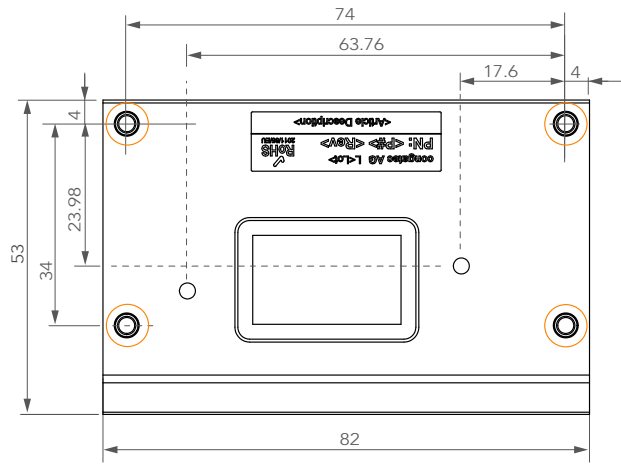



 $\varnothing 2.7 \times 6$ mm
non-threaded standoff
for borehole version

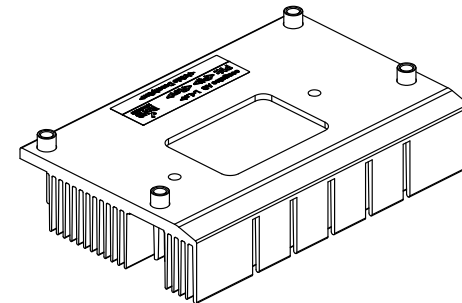
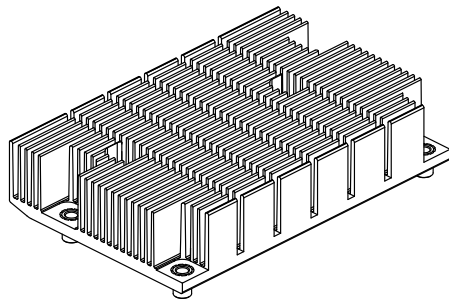
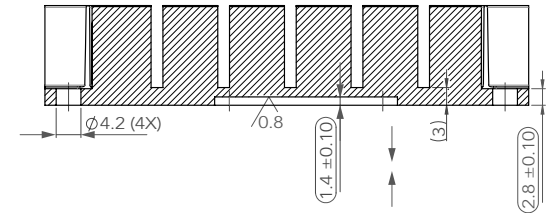


4.2 CSP Dimensions

Bare-die Variants (Commercial)

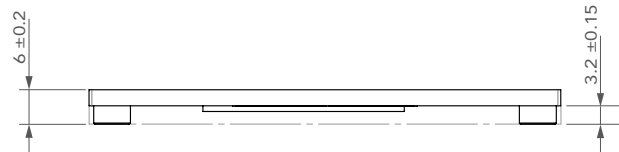
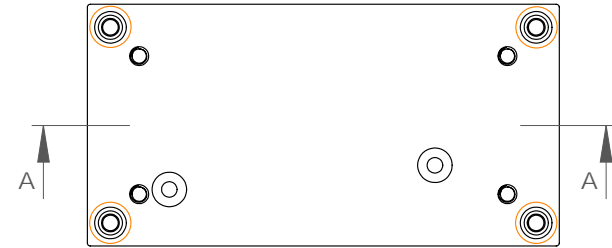
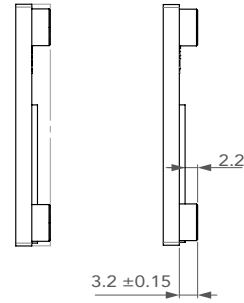
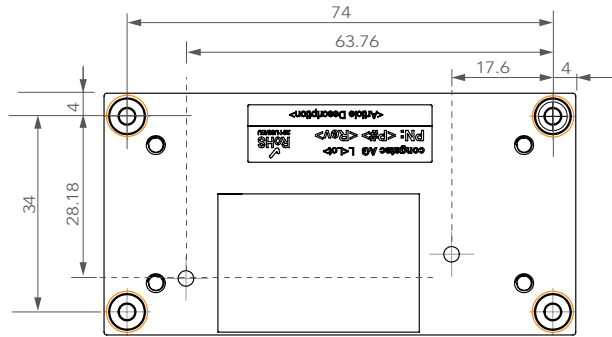




 ø2.7 x 6 mm
 non-threaded standoff
 for borehole version

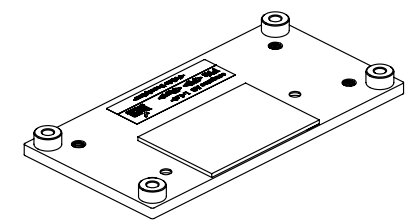
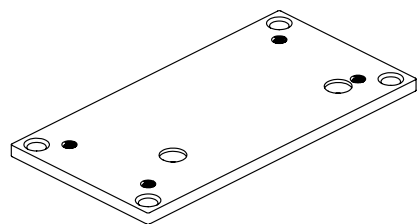
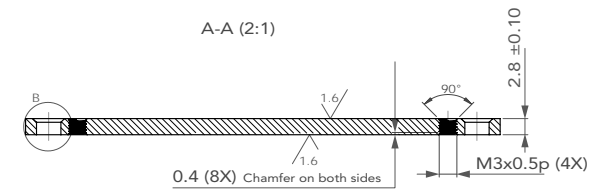


4.3 HSP Dimensions

Lidded Variants (Industrial)

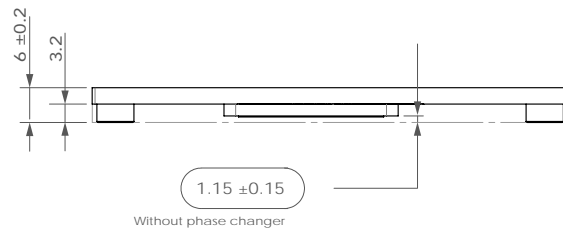
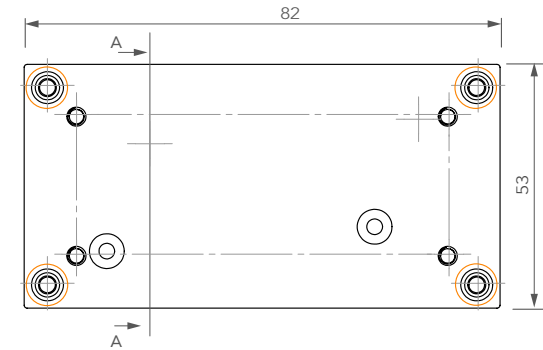
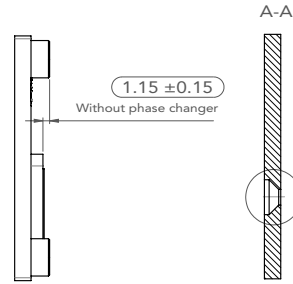
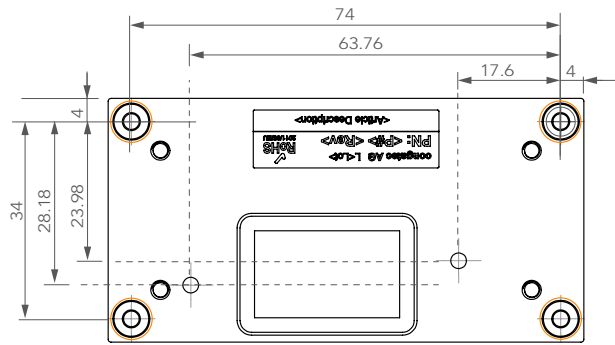



 $\varnothing 2.7 \times 6$ mm non-threaded standoff for borehole version

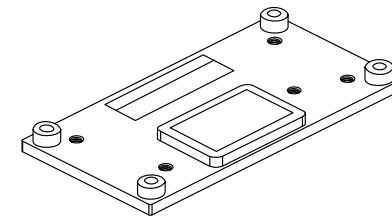
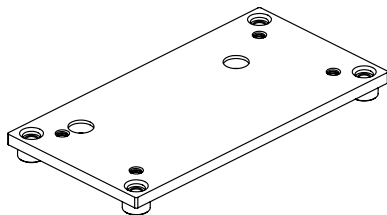
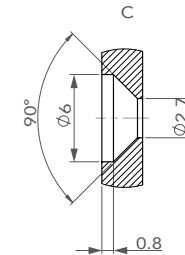


4.4 HSP Dimensions

Bare-die Variants (Commercial)



 $\varnothing 2.7 \times 6$ mm
non-threaded standoff
for borehole version



5 Connector Rows

The conga-SA7 has 314 edge fingers that mate with the MXM3 connector located on the carrier board. This connector is able to interface the signals on the conga-SA7 with the carrier board peripherals.

5.1 PCI Express™

The conga-SA7 offers up to four PCI Express™ lanes. The lanes support:

- up to 8 GT/s (Gen 3) speed
- a 4 x1 link configuration (default) ^{1,3}
- a 1 x4 or 2 x2 or 1 x2 + 2 x1 link ^{2,3} configuration
- lane polarity inversion



Note

- ^{1.} Requires a clock buffer on the carrier board
- ^{2.} Possible only with a custom BIOS firmware
- ^{3.} The conga-SA7 provides PCIe_A_REFCK, PCIe_B_REFCK and PCIe_C_REFCK reference clocks to the carrier board.

5.1.1 Possible Reference Clock Configuration

The conga-SA7 provides three PCIe reference clocks to the carrier board. The possible reference clock configuration is described in the table below.

Table 8 PCIe Reference Clock Configuration

| PCIe Lanes to Carrier Board | Possible Link Configuration | | | | |
|-----------------------------|---------------------------------|-----------------------|------------------------|-----------------|-----------------|
| | Default (4 x1) | Option 1 (2x1 + 1 x2) | Option 2 (1 x2 + 2 x1) | Option 3 (2 x2) | Option 4 (1 x4) |
| PCIe_A | PCIe_A_REFCK | PCIe_A_REFCK | PCIe_A_REFCK | PCIe_A_REFCK | PCIe_A_REFCK |
| PCIe_B | PCIe_B_REFCK | PCIe_B_REFCK | | PCIe_B_REFCK | |
| PCIe_C | PCIe_C_REFCK | PCIe_C_REFCK | PCIe_B_REFCK | PCIe_B_REFCK | |
| PCIe_D | PCIe_C_REFCK via carrier buffer | | PCIe_C_REFCK | | |

5.2 Display Interfaces

The conga-SA7 offers the following display interfaces:

- dual-channel LVDS
- native HDMI
- optional dual-mode DisplayPort (DP++)
- optional eDP or MIPI-DSI

The table below shows the display combination.

Table 9 Display Combination

| | Display 1 (DDI0) | | Display 2 (DDI1) | | Display 3 (DDI2) | |
|----------|--------------------|--|------------------|------------------|------------------|------------------|
| | Interface | Max. Resolution | Interface | Max. Resolution | Interface | Max. Resolution |
| Default | LVDS | 1920x1200 @ 60Hz (dual mode) | DP++ | 4096x2160 @ 60Hz | HDMI | 4096x2160 @ 60Hz |
| Option 1 | eDP or DSI | eDP: 3840x2160 @ 60 Hz DSI: 3200x2000 @ 60 Hz (1 x4 lane) or 4096x2304 @ 60 Hz (2 x4 lane) | DP++ | 4096x2160 @ 60Hz | HDMI | 4096x2160 @ 60Hz |
| Option 2 | LVDS or eDP or DSI | LVDS: 1920x1200 @ 60Hz (dual mode) eDP: 3840x2160 @ 60 Hz DSI: 3200x2000 @ 60 Hz (1 x4 lane) or 4096x2304 @ 60 Hz (2 x4 lane) | DP++ | 4096x2160 @ 60Hz | DP++ | 4096x2160 @ 60Hz |



Note

1. The resolutions in table 9 apply when multiple displays are connected.
2. If eDP is the only active display, the eDP resolution is 4096x2160 @ 60Hz
3. If MIPI-DSI is the only active display, the resolution with compression is 5120x3200 @ 60 Hz.

5.2.1 LVDS

The conga-SA7 offers an LVDS interface. The interface supports the following:

- single- or dual-channel LVDS (color depths of 18 bpp or 24 bpp)
- integrated flat panel interface with clock frequency up to 112 MHz
- VESA and OpenLDI LVDS color mappings
- automatic panel detection via Embedded Panel Interface based on VESA EDID™ 1.3
- resolution up to 1920x1200 in dual LVDS bus mode



Note

1. LVDS channel A (first channel) supports an optional eDP or MIPI-DSI x4 interface (assembly option).
2. Variants with optional eDP or MIPI DSI interface do not support LVDS interface
3. Only one MIPI DSI panel is supported (one channel, with up to four lanes)

5.2.2 HDMI

The conga-SA7 offers a native HDMI interface. The interface supports the following:

- HDMI 2.0b specification
- data rate of 5.94 GT/s
- resolutions up to 4096x2160 @ 60 Hz



Note

1. The HDMI interface supports an optional dual-mode DisplayPort interface (assembly option).
2. Variants with optional dual-mode DisplayPort do not support native HDMI voltage levels.

5.2.3 DP ++

The conga-SA7 offers a dual-mode DisplayPort (DP++). The interface supports:

- VESA DisplayPort standard 1.4
- data rates of 5.4 GT/s without re-timer
- resolutions up to 4096x2160 @ 60 Hz



Note

1. The conga-SA7 offers an optional dual-mode DisplayPort interface (assembly option).
2. Variants with optional dual-mode DisplayPort do not support native HDMI voltage levels.

5.3 SATA

The conga-SA7 offers a SATA interface. The interface supports:

- SATA specification 3.2
- independent DMA operation
- data transfer rates up to 6.0 Gb/s
- AHCI mode using memory space



Note

SATA interface does not support legacy mode using I/O space.

5.4 Gigabit Ethernet

The conga-SA7 offers two Gigabit Ethernet interfaces via TI DP83867CS/IS Ethernet PHY. The interfaces support the following:

- full- or half-duplex operation at 10/100/1000 Mb/s
- precision clock synchronization
- low jitter and latency
- TSN compliancy
- Wake-on-LAN

5.5 USB

The conga-SA7 supports the following:

- up to six USB 2.0 ports
- up to two Superspeed receive and transmit differential pairs for SuperSpeed signaling
- USB 2.0 and 3.1 specification
- up to 480 Mb/s data transfer for USB 2.0
- up to 5 Gb/s for USB 3.1 Gen 1 or up to 10 Gb/s for USB 3.1 Gen 2
- SuperSpeed, high-speed, full-speed and low-speed signaling

The possible options for USB port mapping are shown in table 10.

Table 10 Possible USB Port Mapping

| | USB 2.0 | | USB 3.1 Gen 2/2.0 | |
|----------|-----------|-----------|-------------------|-----------|
| | Host Only | Dual Role | Host Only | Dual Role |
| Default | 4 ports | TBD | 2 port | - |
| Option 1 | 4 ports | - | 2 port | TBD |
| Option 2 | 4 ports | - | 2 ports | - |
| Option 3 | 6 ports | - | - | - |



Note

For USB 3.1 Gen 2 support on your carrier board, pair USB 2.0 port 2 or 3 or both with the SuperSpeed signals.

5.6 Audio (HDA)

The conga-SA7 offers a High Definition Audio interface. The HDA_RST# pin which is multiplexed with GPIO4 is configured to support HD audio by default.



Note

The audio interface will not function if you configure the multiplexed pin for GPIO functionality.

5.7 SD Card

The conga-SA7 offers a 4-bit SD interface. The interface supports:

- SD Memory Card Specification 3.01
- SD 3.01 @ 1.8 V or @ 3.3 V signaling
- up to 200 MHz clock frequency
- up to 100 MB/s data rates with four parallel data lines
- card insertion and removal detection



Note

The SD card interface supports only storage devices.

5.8 UART

The conga-SA7 provides four UART ports:

- UART1 and UART2 via the SoC ¹
- UART0 and UART3 via the congatec board controller ²



Note

¹. *No support for legacy mode operation*

². *Driver is available on the congatec website at www.congatec.com*

5.9 GPIO

The conga-SA7 offers up to 14 GPIOs—11 GPIOs by default and three GPIOs through multiplexed pins P112–P114. The GPIOs are controlled by the congatec Board controller.

If you configure the multiplexed pins (P112–P114) for GPIO functionality, their alternate functions (HDA audio, fan control) will not be available. See Table 31 “GPIO Signal Description” for more information.

5.10 SPI

The conga-SA7 offers two SPI interfaces:

- an eSPI for general purpose SPI devices
- SPI0 for on-module or carrier board flash device



SPI0 can optionally be rerouted for general purpose SPI devices (assembly option).

5.11 I2C

The conga-SA7 offers two I2C interfaces:

- general purpose I2C
- power management I2C

These interfaces are implemented through the congatec board controller and accessed through the congatec CGOS driver and API. The controller provides a fast-mode multi-master I2C bus that has maximum I2C bandwidth.

5.12 Power Control

The conga-SA7 operates only with 5 V input voltage. Its power-up sequence is described below:

1. The 5 V input voltage (VDD_IN) supplied to the carrier board powers the conga-SA7.
2. The conga-SA7 enables its power circuits if the VIN_PWR_BAD# signal is high.
3. Depending on the carrier board design and configuration, the conga-SA7 detects a power button event (PWRBTN#) if implemented.
4. The conga-SA7 enables the carrier board power by asserting CARRIER_PWR_ON (SUS_S5#) and CARRIER_STBY# (SUS_S3#).
5. The conga-SA7 releases the RESET_OUT# and starts the boot process.

The power control signals VIN_PWR_BAD#, CARRIER_PWR_ON, CARRIER_STBY#, RESET_IN#, RESET_OUT# and POWER_BTN# are described below:

VIN_PWR_BAD#

If VIN_PWR_BAD# signal (pin S150) is low, it indicates that the input voltage to the conga-SA7 is either not ready or out of the specified range.



Carrier board hardware should drive this signal low until the input power is up and stable. Releasing VIN_PWR_BAD# too early can cause numerous boot up problems.

CARRIER_PWR_ON

The CARRIER_PWR_ON signal (pin S154) is an active-high output signal. The module asserts this signal when all its power supplies are up, and subsequently enables the carrier board power supplies. This signal is equivalent to ACPI SUS_S5# signal.

CARRIER_STBY#

The CARRIER_STBY# signal (pin S153) is an active-low output that can be used to indicate that the conga-SA7 is going into suspend state, where only power management functions and system memory are powered.

The CARRIER_STBY# signal can also be used to disable the carrier board power that is not required during standby.

RESET_IN#

The RESET_IN# signal (pin P127) is an active-low open drain input signal from the carrier board. The signal may be used to force the module to reset or reboot.

RESET_OUT#

The RESET_OUT# signal (pin P126) is an active-low output signal from the module. The module asserts this signal during the power-up sequencing to allow the carrier board power circuits to come up. The module deasserts this signal to begin the boot-up process.

POWER_BTN#

The POWER_BTN# (pin P128) is an active-low open drain power button input from the carrier board. This power button signal is used to wake up or shut down the system from S5 state (soft off).

Power Supply Implementation Guidelines

The operational power source for the conga-SA7 is 5 V. The remaining necessary voltages are internally generated on the module with onboard voltage regulators.



Note

When designing a power supply for a conga-SA7 application, be aware that the system may malfunction when a 5V power supply that produces non-monotonic voltage is used to power the system up. Though this problem is rare, it has been observed in some mobile power supply applications.

The problem is that some internal circuits on the module (e.g. clock-generator chips) generate their own reset signals when the supply voltage exceeds a certain voltage threshold. A voltage dip after passing this threshold may lead to these circuits becoming confused, thereby resulting in a malfunction.

To ensure this problem does not occur, observe the power supply rise waveform through an oscilloscope, during the power supply qualification phase. This will help to determine if the rise is indeed monotonic and does not have any dips. For more information, see the “Power Supply Design Guide for Desktop Platform Form Factors” document at www.intel.com.

Inrush and Maximum Current Peaks on VDD_IN

The maximum peak-current on the conga-SA7 VDD_IN (5 V) power rail can be as high as 5 A for a maximum of 100 μ s. You should therefore ensure the power supply and decoupling capacitors provide enough power to drive the module.



Note

For more information about power control event signals, refer to the SMARC[®] specification.

6 Additional Features

6.1 Optional Onboard Interfaces

The conga-SA7 offers an optional Wi-fi/Bluetooth module (assembly option).

6.2 eMMC

The conga-SA5 offers an eMMC 5.1 flash onboard. Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology.

The performance of the newer eMMC may vary depending on the eMMC technology.



Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.”

6.3 Security Features

The conga-SA7 offers a discrete TPM 2.0 (Infineon SLB9670VQ2.0) by default.

6.4 congatec Board Controller (cBC)

The conga-SA7 is equipped with a microcontroller. The microcontroller plays an important role for most of the congatec BIOS features. By isolating some of the embedded features such as system monitoring or the I²C bus from the x86 core architecture, the microcontroller increases the performance and reliability of the BIOS features, even during low power mode. In addition, it ensures the congatec embedded feature set is compatible amongst all congatec modules.

Some of the features offered by the cBC are described below:

6.4.1 Board Information

The cBC provides a rich data-set of manufacturing and board information such as serial number, EAN number, hardware and firmware revisions, and so on. It also keeps track of dynamically changing data like runtime meter and boot counter.

6.4.2 General Purpose Input/Output

The conga-SA7 offers general purpose inputs and outputs for custom system design. These GPIOs are controlled by the cBC.

6.4.3 Fan Control

The cBC uses the PWM (FAN_PWMOUT) signal to adjust the rotational speed of the fan without changing the fan's input voltage. Additionally, the FAN_TACHOIN signal provides the ability to monitor the system's fan RPMs (revolutions per minute). For accurate RPM reading, the FAN_TACHOIN signal must receive two pulses per revolution. Therefore, a two pulse per revolution fan or similar hardware solution is recommended.



Note

1. Use a four-wire fan to generate the correct speed readout. For the correct fan control (PWMOUT, TACHIN) implementation, see the SMARC Design Guide Specification.
2. PWMOUT and TACHIN pins are shared with GPIO 5 and 6 respectively. The conga-SA7 does not support fan control if these pins are used for GPIO functionality.

6.4.4 Power Loss Control

The cBC has full control of the power-up of the module and therefore can be used to specify the behavior of the system after an AC power loss condition. Supported modes are "Always On", "Remain Off" and "Last State".

6.4.5 Watchdog

The conga-SA7 is equipped with a multi stage watchdog solution that is triggered by software. The conga-SA7 does not support external hardware triggering because the SMARC Specification does not provide support for external hardware triggering of the watchdog. For more information, see the application note AN3_Watchdog.pdf on the congatec GmbH website at www.congatec.com.



Note

The conga-SA7 module does not support the watchdog NMI mode.

6.4.6 Enhanced Soft-Off State

The conga-SA7 supports an enhanced Soft-Off state (S5e)—a congatec proprietary low-power Soft-Off state. In this state, the CPU module switches off almost all the onboard logic in order to reduce the power consumption to absolute minimum (between 0.05 mA and 0.09 mA).

Refer to congatec application note AN36_Enhanced_Soft_Off.pdf for detailed description of the S5e state.

6.5 OEM BIOS Customization

The conga-SA7 is equipped with congatec Embedded BIOS, which is based on American Megatrends Inc. Aptio UEFI firmware. The congatec Embedded BIOS allows system designers to modify the BIOS. For more information about customizing the congatec Embedded BIOS, refer to the congatec System Utility user's guide CGUTLm1x.pdf on the congatec website at www.congatec.com or contact technical support.

The customizable features are described below:

6.5.1 OEM Default Settings

This feature allows system designers to create and store their own BIOS default configuration. Customized BIOS development by congatec for OEM default settings is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_OEM_Default_Map.pdf on the congatec website for details on how to add OEM default settings to the congatec Embedded BIOS.

6.5.2 OEM Boot Logo

This feature allows system designers to replace the standard text output displayed during POST with their own BIOS boot logo. Customized BIOS development by congatec for OEM Boot Logo is no longer necessary because customers can easily perform this configuration by themselves using the congatec system utility CGUTIL. See congatec application note AN8_Create_And_Add_Bootlogo.pdf on the congatec website for details on how to add OEM boot logo to the congatec Embedded BIOS.

6.5.3 OEM POST Logo

This feature allows system designers to replace the congatec POST logo displayed in the upper left corner of the screen during BIOS POST with their own BIOS POST logo. Use the congatec system utility CGUTIL 1.5.4 or later to replace/add the OEM POST logo.

6.5.4 OEM BIOS Code/Data

With the congatec embedded BIOS, system designers can add their own code to the BIOS POST process. The congatec Embedded BIOS first calls the OEM code before handing over control to the OS loader.



The OEM BIOS code of the new UEFI based firmware is called only when the CSM (Compatibility Support Module) is enabled in the BIOS setup menu. For more information on how to add OEM code, contact congatec technical support.

6.5.5 OEM DXE Driver

This feature allows designers to add their own UEFI DXE driver to the congatec embedded BIOS. Contact congatec technical support for more information on how to add an OEM DXE driver.

6.6 congatec Battery Management Interface

To facilitate the development of battery powered mobile systems based on embedded modules, congatec GmbH defined an interface for the exchange of data between a CPU module (using an ACPI operating system) and a Smart Battery system. A system developed according to the congatec Battery Management Interface Specification can provide the battery management functions supported by an ACPI capable operating system (e.g. charge state of the battery, information about the battery, alarms/events for certain battery states, ...) without the need for any additional modifications to the system BIOS.

In addition to the ACPI-Compliant Control Method Battery mentioned above, the latest versions of the conga-SA7 BIOS and board controller firmware also support LTC1760 battery manager from Linear Technology and a battery only solution (no charger). All three battery solutions are supported on the I2C bus and the SMBus. This gives the system designer more flexibility when choosing the appropriate battery sub-system.

For more information about the supported Battery Management Interface, contact your local sales representative.

6.7 API Support (CGOS)

In order to benefit from the above mentioned non-industry standard feature set, congatec provides an API that allows application software developers to easily integrate all these features into their code. The CGOS API (congatec Operating System Application Programming Interface) is the congatec proprietary API that is available for all commonly used Operating Systems such as Win32, Win64, Win CE, Linux.

The architecture of the CGOS API driver provides the ability to write application software that runs unmodified on all congatec CPU modules. All the hardware related code is contained within the congatec embedded BIOS on the module. See section 1.1 of the CGOS API software developers guide, which is available on the congatec website.

6.8 congatec System Sensors

The conga-SA7 offers the following sensors and monitors:

- temperature sensors
 - CPU temperature based on CPU Digital Thermal Sensor
 - Board temperature sensor located on the Board Controller
- voltage sensors
 - 5V standard voltage sensor
- current sensor
- fan monitor

The sensors and monitors are accessible through CGOS interface, and also visible on the “Health Monitor” submenu in the BIOS Setup.

6.9 Suspend to Ram

The Suspend to RAM feature is available on the conga-SA7.

7 conga Tech Notes

The conga-SA7 has some technological features that require additional explanation. The following section will give the reader a better understanding of some of these features.

7.1 Intel® Elkhart Lake SoC Features

7.1.1 Processor Core

The SoC features Dual or Quad 3-way Superscalar, Out-of-Order Execution processor cores. Some of the features supported by the core are:

- Intel® 64 architecture
- Intel® Streaming SIMD Extensions
- Support for Intel® VTx-2 and VT-d
- Thermal management support via Intel® Thermal Monitor
- Uses Programmable Service Engine Interrupt Routing
- Uses 10 nm process technology



Note

Intel® Hyper-Threading technology is not supported (four cores execute four threads)

7.1.1.1 Intel® Virtualization Technology

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. With this technology, multiple, independent operating systems can run simultaneously on a single system. The technology components support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel® Virtualization Technology for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness.

RTS Real-Time Hypervisor supports Intel® VT and is verified on all current congatec x86 hardware.



Note

congatec supports RTS Hypervisor.

7.1.1.2 AHCI

The SoC provides hardware support for Advanced Host Controller Interface (AHCI), a programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices (each device is treated as a master) and hardware-assisted native command queuing. AHCI also provides usability enhancements such as Hot-Plug.

7.1.1.3 Thermal Management

ACPI is responsible for allowing the operating system to play an important part in the system's thermal management. This results in the operating system having the ability to take control of the operating environment by implementing cooling decisions according to the demands put on the CPU by the application.

The conga-SA7 ACPI thermal solution offers two different cooling policies.

- **Passive Cooling**

When the temperature in the thermal zone must be reduced, the operating system can decrease the power consumption of the processor by throttling the processor clock. One of the advantages of this cooling policy is that passive cooling devices (in this case the processor) do not produce any noise. Use the "passive cooling trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to start or stop the passive cooling procedure.

- **Critical Trip Point**

If the temperature in the thermal zone reaches a critical point then the operating system will perform a system shut down in an orderly fashion in order to ensure that there is no damage done to the system as result of high temperatures. Use the "critical trip point" setup node in the BIOS setup program to determine the temperature threshold that the operating system will use to shut down the system.



Note

The end user must determine the cooling preferences for the system by using the setup nodes in the BIOS setup program to establish the appropriate trip points.

If passive cooling is activated and the processor temperature is above the trip point the processor clock is throttled. See section 12 of the ACPI Specification 2.0 C for more information about passive cooling.

7.2 ACPI Suspend Modes and Resume Events

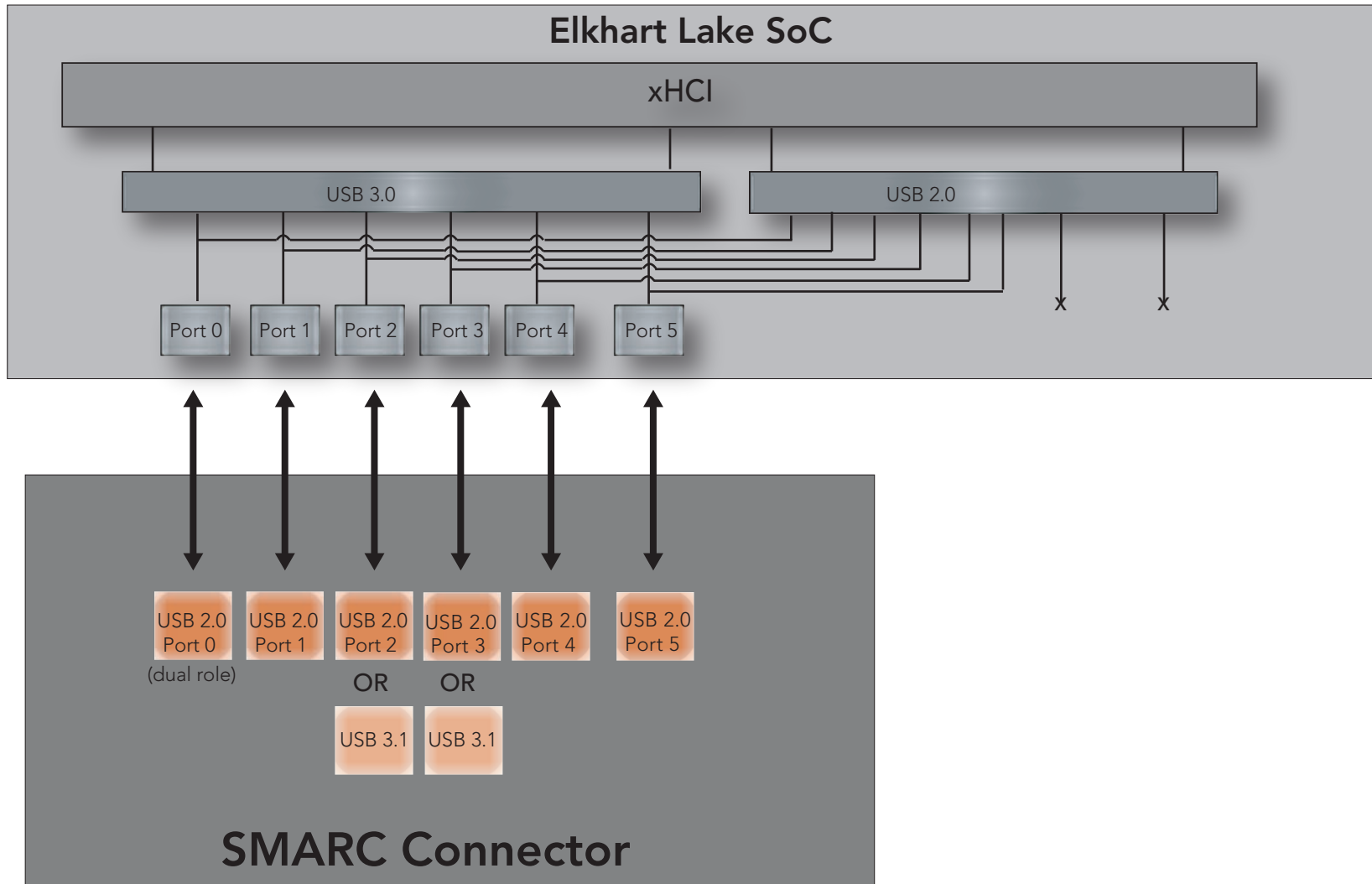
The conga-SA7 BIOS supports S3 (Suspend to RAM). The BIOS does not support S4 (Suspend to Disk).

Table 11 Wake Events

The table below lists the events that wake the system from S3.

| Wake Event | Conditions or remarks |
|-----------------------------|--|
| Power Button | Wakes unconditionally from S3 |
| Onboard LAN Event | Device driver must be configured for Wake On LAN support |
| SMBALERT# | Wakes unconditionally from S3 |
| PCI Express WAKE# | Wakes unconditionally from S3 |
| WAKE# | Wakes unconditionally from S3 |
| USB Mouse/Keyboard Event | When standby mode is set to S3, the standby power source must power the USB hardware: <ul style="list-style-type: none">• in the ACPI setup menu, set "USB Device Wakeup" to "Enabled" (if setup node is available in the BIOS setup menu)• in Device Manager, expand "Keyboard" or "Mice and other pointing devices"• right-click keyboard or mouse device and click "Properties"• click "Power Management" tab and check "Allow this device to wake the computer" |
| RTC Alarm | In the power setup menu, active and configure "Resume On RTC Alarm" |
| Watchdog Power Button Event | Wakes unconditionally from S3 |

7.3 USB Port Mapping



8 Signal Descriptions and Pinout Tables

The following section describes the signals found on SMARC® module's edge fingers. The pinout of the module complies with SMARC Specification 2.1.

The table below describes the terminology used in this section. The PU/PD column indicates if a pull-up or pull-down resistor has been used. If the field entry area in this column for the signal is empty, then no pull-up or pull-down resistor has been implemented. The “#” symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level.



Not all the signals described in this section are available on all conga-SA7 variants. Use the article number of the module and refer to the “conga-SA7 Options Information” table in section 1 to determine the options available on the module.

Table 12 Signal Tables Terminology Descriptions

| Term | Description |
|-------------|--|
| I | Input to the module |
| O | Output from the module |
| O OD | Open drain output from the module |
| I OD | Open drain input to the module, with pull-up on module |
| OD | Open drain |
| I/O | Bi-directional Input/Output Pin |
| PU(i)/PD(i) | Pull-up or pull-down resistor internal to the SoC or transceiver |
| VDD_IN | Signal may be exposed to module input voltage range (4.75 to 5.25V) |
| CMOS | Logic input or output with 3.3 V signal level |
| GBe MDI | Differential analog signaling for Gigabit Media Dependent Interface |
| LVDS DP | LVDS signaling for DisplayPort devices |
| LVDS D-PHY | LVDS signaling for MIPI CSI-2 camera and DSI display interfaces |
| LVDS LCD | LVDS signaling for LVDS LCD displays |
| LVDS PCIE | LVDS signaling for PCIe interfaces |
| LVDS SATA | LVDS signaling for SATA interfaces |
| TMDS | LVDS signaling for HDMI display interfaces |
| USB | DC coupled differential signaling for traditional (non-Superspeed) USB signals |
| USB SS | LVDS signaling for SuperSpeed USB signals |
| PCIE | PCI Express differential pair signals. In compliance with the PCI Express Base Specification 2.0 |
| USB VBUS 5V | 5V tolerant input for USB VBUS detection |

Table 13 SMARC Edge Finger Pinout

| P-PIN | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|-------------------------|-------|--------------------------------------|
| | | S1 | CSI1_TX+ / I2C_CAM1_CK ² |
| P1 | SMB_ALERT# | S2 | CSI1_TX- / I2C_CAM1_DAT ² |
| P2 | GND | S3 | GND |
| P3 | CSI1_CK+ ² | S4 | RSVD ² |
| P4 | CSI1_CK- ² | S5 | CSI0_TX+ / I2C_CAM0_CK |
| P5 | GBE1_SDP | S6 | CAM_MCK ² |
| P6 | GBE0_SDP | S7 | CSI0_TX- / I2C_CAM0_DAT |
| P7 | CSI1_RX0+ ² | S8 | CSI0_CK+ ² |
| P8 | CSI1_RX0- ² | S9 | CSI0_CK- ² |
| P9 | GND | S10 | GND |
| P10 | CSI1_RX1+ ² | S11 | CSI0_RX0+ ² |
| P11 | CSI1_RX1- ² | S12 | CSI0_RX0- ² |
| P12 | GND | S13 | GND |
| P13 | CSI1_RX2+ ² | S14 | CSI0_RX1+ ² |
| P14 | CSI1_RX2- ² | S15 | CSI0_RX1- ² |
| P15 | GND | S16 | GND |
| P16 | CSI1_RX3+ ² | S17 | GBE1_MDIO+ |
| P17 | CSI1_RX3- ² | S18 | GBE1_MDIO- |
| P18 | GND | S19 | GBE1_LINK100# |
| P19 | GBE0_MDI3- | S20 | GBE1_MDI1+ |
| P20 | GBE0_MDI3+ | S21 | GBE1_MDI1- |
| P21 | GBE0_LINK100# | S22 | GBE1_LINK1000# |
| P22 | GBE0_LINK1000# | S23 | GBE1_MDI2+ |
| P23 | GBE0_MDI2- | S24 | GBE1_MDI2- |
| P24 | GBE0_MDI2+ | S25 | GND |
| P25 | GBE0_LINK_ACT# | S26 | GBE1_MDI3+ |
| P26 | GBE0_MDI1- | S27 | GBE1_MDI3- |
| P27 | GBE0_MDI1+ | S28 | GBE1_CTREF ² |
| P28 | GBE0_CTREF ² | S29 | PCIE_D_TX+ / SERDES_0_TX+ |
| P29 | GBE0_MDI0- | S30 | PCIE_D_TX- / SERDES_0_TX- |
| P30 | GBE0_MDI0+ | S31 | GBE1_LINK_ACT# |
| P31 | SPI0_CS1# | S32 | PCIE_D_RX+ / SERDES_0_RX+ |

| P-PIN | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|-----------------------------------|-------|----------------------------|
| P32 | GND | S33 | PCIE_D_RX- / SERDES_0_RX- |
| P33 | SDIO_WP | S34 | GND |
| P34 | SDIO_CMD | S35 | USB4+ |
| P35 | SDIO_CD# | S36 | USB4- |
| P36 | SDIO_CK | S37 | USB3_VBUS_DET ¹ |
| P37 | SDIO_PWR_EN | S38 | AUDIO_MCK |
| P38 | GND | S39 | I2S0_LRCK ¹ |
| P39 | SDIO_D0 | S40 | I2S0_SDOOUT ¹ |
| P40 | SDIO_D1 | S41 | I2S0_SDIN ¹ |
| P41 | SDIO_D2 | S42 | I2S0_CK ¹ |
| P42 | SDIO_D3 | S43 | ESPI_ALERT0# |
| P43 | SPI0_CS0# | S44 | ESPI_ALERT1# |
| P44 | SPI0_CK | S45 | MDIO_CLK ² |
| P45 | SPI0_DIN | S46 | MDIO_DAT ² |
| P46 | SPI0_DO | S47 | GND |
| P47 | GND | S48 | I2C_GP_CK |
| P48 | SATA_TX+ | S49 | I2C_GP_DAT |
| P49 | SATA_TX- | S50 | HDA_SYNC |
| P50 | GND | S51 | HDA_SDO |
| P51 | SATA_RX+ | S52 | HDA_SDI |
| P52 | SATA_RX- | S53 | HDA_CK |
| P53 | GND | S54 | SATA_ACT# |
| P54 | ESPI_CS0# / SPI1_CS0# / QSPI_CS0# | S55 | USB5_EN_OC# |
| P55 | ESPI_CS1# / SPI1_CS1# / QSPI_CS1# | S56 | ESPI_IO_2 / QSPI_IO_2 |
| P56 | ESPI_CK / SPI1_CK / QSPI_CK | S57 | ESPI_IO_3 / QSPI_IO_3 |
| P57 | ESPI_IO_1 / SPI1_DIN / QSPI_IO_1 | S58 | ESPI_RESET# |
| P58 | ESPI_IO_0 / SPI1_DO / QSPI_IO_0 | S59 | USB5+ |
| P59 | GND | S60 | USB5- |
| P60 | USB0+ | S61 | GND |
| P61 | USB0- | S62 | USB3_SSTX+ |
| P62 | USB0_EN_OC# | S63 | USB3_SSTX- |
| P63 | USB0_VBUS_DET ¹ | S64 | GND |
| P64 | USB0_OTG_ID ¹ | S65 | USB3_SSRX+ |
| P65 | USB1+ | S66 | USB3_SSRX- |

| P-PIN | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|-----------------------|-------|---------------------------|
| P66 | USB1- | S67 | GND |
| P67 | USB1_EN_OC# | S68 | USB3+ |
| P68 | GND | S69 | USB3- |
| P69 | USB2+ | S70 | GND |
| P70 | USB2- | S71 | USB2_SSTX+ |
| P71 | USB2_EN_OC# | S72 | USB2_SSTX- |
| P72 | RSVD ² | S73 | GND |
| P73 | RSVD ² | S74 | USB2_SSRX+ |
| P74 | USB3_EN_OC# | S75 | USB2_SSRX- |
| | Key | | Key |
| P75 | PCIE_A_RST# | S76 | PCIE_B_RST# |
| P76 | USB4_EN_OC# | S77 | PCIE_C_RST# |
| P77 | PCIE_B_CKREQ# | S78 | PCIE_C_RX+ / SERDES_1_RX+ |
| P78 | PCIE_A_CKREQ# | S79 | PCIE_C_RX- / SERDES_1_RX- |
| P79 | GND | S80 | GND |
| P80 | PCIE_C_REFCK+ | S81 | PCIE_C_TX+ / SERDES_1_TX+ |
| P81 | PCIE_C_REFCK- | S82 | PCIE_C_TX- / SERDES_1_TX- |
| P82 | GND | S83 | GND |
| P83 | PCIE_A_REFCK+ | S84 | PCIE_B_REFCK+ |
| P84 | PCIE_A_REFCK- | S85 | PCIE_B_REFCK- |
| P85 | GND | S86 | GND |
| P86 | PCIE_A_RX+ | S87 | PCIE_B_RX+ |
| P87 | PCIE_A_RX- | S88 | PCIE_B_RX- |
| P88 | GND | S89 | GND |
| P89 | PCIE_A_TX+ | S90 | PCIE_B_TX+ |
| P90 | PCIE_A_TX- | S91 | PCIE_B_TX- |
| P91 | GND | S92 | GND |
| P92 | HDMI_D2+ / DP1_LANE0+ | S93 | DP0_LANE0+ |
| P93 | HDMI_D2- / DP1_LANE0- | S94 | DP0_LANE0- |
| P94 | GND | S95 | DP0_AUX_SEL |
| P95 | HDMI_D1+ / DP1_LANE1+ | S96 | DP0_LANE1+ |
| P96 | HDMI_D1- / DP1_LANE1- | S97 | DP0_LANE1- |

| P-PIN | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|--------------------------|-------|-----------------------------------|
| P97 | GND | S98 | DP0_HPD |
| P98 | HDMI_D0+ / DP1_LANE2+ | S99 | DP0_LANE2+ |
| P99 | HDMI_D0- / DP1_LANE2- | S100 | DP0_LANE2- |
| P100 | GND | S101 | GND |
| P101 | HDMI_CK+ / DP1_LANE3+ | S102 | DP0_LANE3+ |
| P102 | HDMI_CK- / DP1_LANE3- | S103 | DP0_LANE3- |
| P103 | GND | S104 | USB3_OTG_ID ¹ |
| P104 | HDMI_HPD / DP1_HPD | S105 | DP0_AUX+ |
| P105 | HDMI_CTRL_CK / DP1_AUX+ | S106 | DP0_AUX- |
| P106 | HDMI_CTRL_DAT / DP1_AUX- | S107 | LCD1_BKLT_EN ² |
| P107 | DP1_AUX_SEL | S108 | LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+ |
| P108 | GPIO0 / CAM0_PWR# | S109 | LVDS1_CK- / eDP1_AUX- / DSI1_CLK- |
| P109 | GPIO1 / CAM1_PWR# | S110 | GND |
| P110 | GPIO2 / CAM0_RST# | S111 | LVDS1_0+ / eDP1_TX0+ / DSI1_D0+ |
| P111 | GPIO3 / CAM1_RST# | S112 | LVDS1_0- / eDP1_TX0- / DSI1_D0- |
| P112 | GPIO4 / HDA_RST# | S113 | eDP1_HPD / DSI1_TE ² |
| P113 | GPIO5 / PWM_OUT | S114 | LVDS1_1+ / eDP1_TX1+ / DSI1_D1+ |
| P114 | GPIO6 / TACHIN | S115 | LVDS1_1- / eDP1_TX1- / DSI1_D1- |
| P115 | GPIO7 | S116 | LCD1_VDD_EN ² |
| P116 | GPIO8 | S117 | LVDS1_2+ / eDP1_TX2+ / DSI1_D2+ |
| P117 | GPIO9 | S118 | LVDS1_2- / eDP1_TX2- / DSI1_D2- |
| P118 | GPIO10 | S119 | GND |
| P119 | GPIO11 | S120 | LVDS1_3+ / eDP1_TX3+ / DSI1_D3+ |
| P120 | GND | S121 | LVDS1_3- / eDP1_TX3- / DSI1_D3- |
| P121 | I2C_PM_CK | S122 | LCD1_BKLT_PWM ² |
| P122 | I2C_PM_DAT | S123 | GPIO13 |
| P123 | BOOT_SEL0# | S124 | GND |
| P124 | BOOT_SEL1# | S125 | LVDS0_0+ / eDP0_TX0+ / DSI0_D0+ |
| P125 | BOOT_SEL2# | S126 | LVDS0_0- / eDP0_TX0- / DSI0_D0- |
| P126 | RESET_OUT# | S127 | LCD0_BKLT_EN |
| P127 | RESET_IN# | S128 | LVDS0_1+ / eDP0_TX1+ / DSI0_D1+ |
| P128 | POWER_BTN# | S129 | LVDS0_1- / eDP0_TX1- / DSI0_D1- |
| P129 | SER0_TX | S130 | GND |
| P130 | SER0_RX | S131 | LVDS0_2+ / eDP0_TX2+ / DSI0_D2+ |

| P-PIN | Primary (Top) Side | S-Pin | Secondary (Bottom) Side |
|-------|--------------------|-------|-----------------------------------|
| P131 | SER0_RTS# | S132 | LVDS0_2- / eDP0_TX2- / DSI0_D2- |
| P132 | SER0_CTS# | S133 | LCD0_VDD_EN |
| P133 | GND | S134 | LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+ |
| P134 | SER1_TX | S135 | LVDS0_CK- / eDP0_AUX- / DSI0_CLK- |
| P135 | SER1_RX | S136 | GND |
| P136 | SER2_TX | S137 | LVDS0_3+ / eDP0_TX3+ / DSI0_D3+ |
| P137 | SER2_RX | S138 | LVDS0_3- / eDP0_TX3- / DSI0_D3- |
| P138 | SER2_RTS# | S139 | I2C_LCD_CK |
| P139 | SER2_CTS# | S140 | I2C_LCD_DAT |
| P140 | SER3_TX | S141 | LCD0_BKLT_PWM |
| P141 | SER3_RX | S142 | GPIO12 |
| P142 | GND | S143 | GND |
| P143 | CAN0_TX | S144 | eDP0_HPD / DSI0_TE |
| P144 | CAN0_RX | S145 | WDT_TIME_OUT# |
| P145 | CAN1_TX | S146 | PCIE_WAKE# |
| P146 | CAN1_RX | S147 | VDD_RTC |
| P147 | VDD_IN | S148 | LID# |
| P148 | VDD_IN | S149 | SLEEP# |
| P149 | VDD_IN | S150 | VIN_PWR_BAD# |
| P150 | VDD_IN | S151 | CHARGING# |
| P151 | VDD_IN | S152 | CHARGER_PRSNT# |
| P152 | VDD_IN | S153 | CARRIER_STBY# |
| P153 | VDD_IN | S154 | CARRIER_PWR_ON |
| P154 | VDD_IN | S155 | FORCE_RECOV# |
| P155 | VDD_IN | S156 | BATLOW# |
| P156 | VDD_IN | S157 | TEST# |
| | | S158 | GND |

 **Note**

1. *Not supported*
2. *Not connected*

Table 14 LVDS Signal Description

| Signals | Pins | Description | I/O | PU/PD | Comments |
|------------------------|--------------|--|----------------|--------|---------------|
| LVDS0_0+ LVDS0_0- | S125 S126 | LVDS primary data channel, differential pair 0 | O LVDS LCD | | |
| LVDS0_1+ LVDS0_1- | S128 S129 | LVDS primary data channel, differential pair 1 | O LVDS LCD | | |
| LVDS0_2+ LVDS0_2- | S131 S132 | LVDS primary data channel, differential pair 2 | O LVDS LCD | | |
| LVDS0_3+ LVDS0_3- | S137 S138 | LVDS primary data channel, differential pair 3 | O LVDS LCD | | |
| LVDS0_CK+ LVDS0_CK- | S134 S135 | LVDS primary data channel differential clock pair | O LVDS LCD | | |
| LCD0_VDD_EN | S133 | LVDS primary channel power enable. High enables panel VDD | O 1.8V | | |
| LCD0_BKLT_EN | S127 | LVDS primary channel backlight enable. High enables panel backlight | O 1.8V | | |
| LCD0_BKLT_PWM | S141 | LVDS primary channel brightness via pulse width modulation (PWM) | O 1.8V | | |
| LVDS1_0+ LVDS1_0- | S111 S112 | LVDS secondary data channel, differential pair 0 | O LVDS LCD | | |
| LVDS1_1+ LVDS1_1- | S114 S115 | LVDS secondary data channel, differential pair 1 | O LVDS LCD | | |
| LVDS1_2+ LVDS1_2- | S117 S118 | LVDS secondary data channel, differential pair 2 | O LVDS LCD | | |
| LVDS1_3+ LVDS1_3- | S120 S121 | LVDS secondary data channel, differential pair 3 | O LVDS LCD | | |
| LVDS1_CK+ LVDS1_CK- | S108 S109 | LVDS secondary data channel differential clock pair | O LVDS LCD | | |
| LCD1_VDD_EN | S116 | LVDS secondary channel power enable. High enables panel VDD | O 1.8V | | Not connected |
| LCD1_BKLT_EN | S107 | LVDS secondary channel backlight enable. High enables panel backlight | O 1.8V | | |
| LCD1_BKLT_PWM | S122 | LVDS secondary channel brightness control via pulse width modulation (PWM) | O 1.8V | | |
| I2C_LCD_DAT | S140 | DDC data line for flat panel detection and control. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented. | I/O OD 1.8V | PU 2k2 | |
| I2C_LCD_CK | S139 | DDC clock line for flat panel detection and control | O OD 1.8V | PU 2k2 | |

Table 14.1 **Optional eDP Signal Description**

| Signals | Pins | Description | I/O | PU/PD | Comments |
|------------------------|--------------|--|----------------|---------|--|
| eDP0_TX0+ eDP0_TX0- | S125 S126 | eDP0 primary differential data pair 0 | O LVDS DP | | Not supported by default. AC coupling required off-module |
| eDP0_TX1+ eDP0_TX1- | S128 S129 | eDP0 primary differential data pair 1 | O LVDS DP | | |
| eDP0_TX2+ eDP0_TX2- | S131 S132 | eDP0 primary differential data pair 2 | O LVDS DP | | |
| eDP0_TX3+ eDP0_TX3- | S137 S138 | eDP0 primary differential data pair 3 | O LVDS DP | | |
| eDP0_AUX+ eDP0_AUX- | S134 S135 | eDP0 primary auxiliary differential pair for link management and device control | O LVDS DP | | |
| LCD0_VDD_EN | S133 | Primary panel power enable. High enables panel VDD | O 1.8V | | |
| LCD0_BKLT_EN | S127 | Primary backlight enable. High enables panel backlight | O 1.8V | | |
| LCD0_BKLT_PWM | S141 | Primary backlight brightness control via pulse width modulation (PWM) | O 1.8V | | |
| eDP0_HPD | S144 | eDP0 Hot Plug Detect pins for primary eDP display | I 1.8V | PD 100k | 100k PD present only on variants with eDP support |
| eDP1_TX0+ eDP1_TX0- | S111 S112 | eDP1 secondary differential data pair 0 | O LVDS DP | | Not supported |
| eDP1_TX1+ eDP1_TX1- | S114 S115 | eDP1 secondary differential data pair 1 | O LVDS DP | | |
| eDP1_TX2+ eDP1_TX2- | S117 S118 | eDP1 secondary differential data pair 2 | O LVDS DP | | |
| eDP1_TX3+ eDP1_TX3- | S120 S121 | eDP1 secondary differential data pair 3 | O LVDS DP | | |
| eDP1_AUX+ eDP1_AUX- | S108 S109 | eDP1 secondary auxiliary differential pair for link management and device control | O LVDS DP | | |
| LCD1_VDD_EN | S116 | Secondary panel power enable. High enables panel VDD | O 1.8V | | Not connected |
| LCD1_BKLT_EN | S107 | Secondary panel backlight enable. High enables panel backlight | O 1.8V | | |
| LCD1_BKLT_PWM | S122 | Secondary panel backlight brightness control via pulse width modulation (PWM) | O 1.8V | | |
| eDP1_HPD | S113 | eDP1 Hot Plug Detect pins | I 1.8V | | |
| I2C_LCD_DAT | S140 | I2C data to read LCD display EDID EEPROMs. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented | I/O OD 1.8V | PU 1k3 | Optional - eDP panel information is usually via the eDP auxiliary pair |
| I2C_LCD_CLK | S139 | I2C clock to read LCD display EDID EEPROMs | O 1.8V | PU 1k3 | Optional - eDP panel information is usually via the eDP auxiliary pair |

Table 14.2 Optional MIPI-DSI Signal Description

| Signals | Pins | Description | I/O | PU/PD | Comments |
|------------------------|--------------|---|-----------------|--------|--------------------------|
| DSI0_D0+ DSI0_D0- | S125 S126 | DSI0 primary differential data pair 0 | O LVDS D-PHY | | Not supported by default |
| DSI0_D1+ DSI0_D1- | S128 S129 | DSI0 primary differential data pair 1 | O LVDS D-PHY | | |
| DSI0_D2+ DSI0_D2- | S131 S132 | DSI0 primary differential data pair 2 | O LVDS D-PHY | | |
| DSI0_D3+ DSI0_D3- | S137 S138 | DSI0 primary differential data pair 3 | O LVDS D-PHY | | |
| DSI0_CLK+ DSI0_CLK- | S134 S135 | DSI0 primary differential clock pair | O LVDS D-PHY | | |
| DSI0_TE | S144 | DSI0 primary panel tearing effect signal | I 1.8V | | |
| LCD0_VDD_EN | S133 | Primary panel power enable. High enables panel VDD | O 1.8V | | |
| LCD0_BKLT_EN | S127 | Primary panel backlight enable. High enables panel backlight | O 1.8V | | |
| LCD0_BKLT_PWM | S141 | Primary panel backlight brightness control via pulse width modulation (PWM) | O 1.8V | | |
| DSI1_D0+ DSI1_D0- | S111 S112 | DSI1 secondary differential data pair 0 | O LVDS D-PHY | | |
| DSI1_D1+ DSI1_D1- | S114 S115 | DSI1 secondary differential data pair 1 | O LVDS D-PHY | | |
| DSI1_D2+ DSI1_D2- | S117 S118 | DSI1 secondary differential data pair 2 | O LVDS D-PHY | | |
| DSI1_D3+ DSI1_D3- | S120 S121 | DSI1 secondary differential data pair 3 | O LVDS D-PHY | | |
| DSI1_CLK+ DSI1_CLK- | S108 S109 | DSI1 secondary differential clock pair | O LVDS D-PHY | | |
| LCD1_VDD_EN | S116 | Secondary panel power enable. High enables panel VDD | O 1.8V | | |
| LCD1_BKLT_EN | S107 | Secondary panel backlight enable. High enables panel backlight | O 1.8V | | |
| LCD1_BKLT_PWM | S122 | Secondary panel backlight brightness via pulse width modulation (PWM) | O 1.8V | | |
| DSI1_TE | S113 | DSI1 secondary panel tearing effect signal | I 1.8V | | |
| I2C_LCD_DAT | S140 | DDC data line for flat panel detection and control. Possible EDID EEPROM address conflicts may occur if multiple displays are implemented | I/O OD 1.8V | PU 2k2 | |
| I2C_LCD_CLK | S139 | DC clock line for flat panel detection and control | O 1.8V | PU 2k2 | |

 **Note**

The MIPI-DSI interface is not supported by default (assembly option only).

Table 15 HDMI Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|----------------------|--------------|--|-------------|---------|--|
| HDMI_D0+ HDMI_D0- | P98 P99 | TMDS / HDMI differential data pair 0 | O TMDS | | |
| HDMI_D1+ HDMI_D1- | P95 P96 | TMDS / HDMI differential data pair 1 | O TMDS | | |
| HDMI_D2+ HDMI_D2- | P92 P93 | TMDS / HDMI differential data pair 2 | O TMDS | | |
| HDMI_CK+ HDMI_CK- | P101 P102 | TMDS / HDMI differential clock pair | O TMDS | | |
| HDMI_CTRL_CK | P105 | I2C clock line dedicated to HDMI | O 1.8V OD | PU 100k | Level shifter FET and 5V PU resistor shall be placed between the module and the HDMI connector |
| HDMI_CTRL_DAT | P106 | I2C data line dedicated to HDMI | I/O 1.8V OD | PU 100k | |
| HDMI_HPD | P104 | HDMI Hot plug active high detection signal that serves as an interrupt request | I 1.8V | PD 1M | |



Note

For HDMI operation, drive DP1_AUX_SEL (pin P107) to 1.8 V on the carrier board.

Table 15.1 DP++ Operation Over HDMI Pins Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|--------------------------|--------------|---|-------------|---------|-----------------------|
| DP1_LANE0+ DP1_LANE0- | P92 P93 | DisplayPort differential data pair 0 | LVDS DP | | AC coupled off module |
| DP1_LANE1+ DP1_LANE1- | P95 P96 | DisplayPort differential data pair 1 | LVDS DP | | |
| DP1_LANE2+ DP1_LANE2- | P98 P99 | DisplayPort differential data pair 2 | LVDS DP | | |
| DP1_LANE3+ DP1_LANE3- | P101 P102 | DisplayPort differential data pair 3 | LVDS DP | | |
| DP1_HPD | P104 | DisplayPort Hot Plug Detect | I 1.8V | PD 1M | |
| DP1_AUX+ DP1_AUX- | P105 P106 | DisplayPort auxiliary differential pair. Used for link management and device control | I/O 1.8V OD | PD 100k | AC coupled on module |
| | | | | PU 100k | |
| DP1_AUX_SEL | P107 | Pull to GND on carrier for DP operation in dual-mode (DP++) implementations. Drive to 1.8V on carrier for HDMI operation. Terminated on module through 1M resistor to GND | I 1.8V | PD 1M | |



Note

The conga-SA7 offers this interface as an assembly option.

Table 16 DisplayPort++

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|--------------------------|--------------|--|-----------|---------|-----------------------|
| DPO_LANE0+ DPO_LANE0- | S93 S94 | DisplayPort differential data pair 0 | LVDS DP | | AC coupled off module |
| DPO_LANE1+ DPO_LANE1- | S96 S97 | DisplayPort differential data pair 1 | LVDS DP | | |
| DPO_LANE2+ DPO_LANE2- | S99 S100 | DisplayPort differential data pair 2 | LVDS DP | | |
| DPO_LANE3+ DPO_LANE3- | S102 S103 | DisplayPort differential data pair 3 | LVDS DP | | |
| DPO_HPD | S98 | DisplayPort Hot Plug Detect | I 1.8V | PD 1M | |
| DPO_AUX+ | S105 | DisplayPort auxiliary differential pair. Used for link management and device control | LVDS PCIE | PD 100k | AC coupled on module |
| DPO_AUX- | S106 | | LVDS PCIE | PU 100k | |
| DPO_AUX_SEL | S95 | Pulled to GND on carrier for DP operation in dual-mode (DP++) implementations | I 1.8V | PD 1M | |

Table 17 MIPI CSI-2/-3

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|----------------------------|------------|--|-----------------|--------|--------------------|
| CSI0_RX0+ CSI0_RX0- | S11 S12 | CSI0 differential data pair 0 | I LVDS D-PHY | | Not connected |
| CSI0_RX1+ CSI0_RX1- | S14 S15 | CSI0 differential data pair 1 | I LVDS D-PHY | | |
| CSI0_CK+ CSI0_CK- | S8 S9 | CSI0 differential clock pair | I LVDS D-PHY | | |
| CAM0_PWR# / GPIO0 | P108 | Camera 0 power enable, active low output/ General Purpose Input Output 0 | I/O 1.8V | | Supports only GPIO |
| CAM0_RST# / GPIO2 | P110 | Camera 0 reset, active low output / General Purpose Input Output 2 | I/O 1.8V | | |
| I2C_CAM0_CK / CSI0_TX+ | S5 | I2C clock (serial camera support link for serial cameras). | I/O OD 1.8V | PU 2k2 | |
| I2C_CAM0_DAT / CSI0_TX- | S7 | I2C data (serial camera support link for serial cameras) | I/O OD 1.8V | PU 2k2 | |
| CSI1_RX0+ CSI1_RX0- | P7 P8 | CSI1 differential data pair 0 | I LVDS D-PHY | | Not connected |

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|----------------------------|------------|--|-----------------|-------|--------------------|
| CSI1_RX1+ CSI1_RX1- | P10 P11 | CSI1 differential data pair 1 | I LVDS D-PHY | | Not connected |
| CSI1_RX2+ CSI1_RX2- | P13 P14 | CSI1 differential data pair 2 | I LVDS D-PHY | | |
| CSI1_Rx3+ CSI1_RX3- | P16 P17 | CSI1 differential data pair 3 | I LVDS D-PHY | | |
| CSI1_CK+ CSI1_CK- | P3 P4 | CSI1 differential clock pair | I LVDS D-PHY | | |
| CAM1_PWR# / GPIO1 | P109 | Camera 1 power enable, active low output / General Purpose Input Output 1 | I/O 1.8V | | Supports only GPIO |
| CAM1_RST# / GPIO3 | P111 | Camera 1 reset, active low output / General Purpose Input Output 3 | I/O 1.8V | | |
| CAM_MCK | S6 | Master clock output for CSI camera support. May be used for CSI0 or CSI1 or both | O 1.8V | | Not connected |
| I2C_CAM1_CK / CSI1_TX+ | S1 | I2C clock (serial camera support link for serial cameras) | I/O OD 1.8V | | |
| I2C_CAM1_DAT / CSI1_TX- | S2 | I2C data (serial camera support link for serial cameras) | I/O OD 1.8V | | |

Table 18 SDIO Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|--|--------------------------|--|-----------|---------|---------|
| SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3 | P39 P40 P41 P42 | SDIO Data lines | I/O 3.3V | | |
| SDIO_CMD | P34 | SDIO Command/Response. This signal is used for card initialization and for command transfers | I/O 3.3V | | |
| SDIO_CK | P36 | SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs | O 3.3V | | |
| SDIO_WP | P33 | SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards | I OD 3.3V | PU 10k | |
| SDIO_CD# | P35 | SDIO Card Detect. This signal indicates when a SDIO/MMC card is present | I OD 3.3V | PU 10k | |
| SDIO_PWR_EN | P37 | SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device | O 3.3V | PD 100k | |

Table 19 SPI0 Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|-----------|-------|--|--------|---------|---------|
| SPI0_CS0# | P43 | SPI0 master chip select 0 output for selecting SPI boot device | O 1.8V | PU 100k | |
| SPI0_CS1# | P31 | SPI0 master chip select output for selecting the second chip select when two devices are used. Do not use when only one SPI device is used | O 1.8V | | |
| SPI0_CK | P44 | SPI0 master clock output | O 1.8V | PD 75k | |
| SPI0_DIN | P45 | SPI0 master data input (SPI serial input data from the SPI device to SMARC® module) | I 1.8V | | |
| SPI0_DO | P46 | SPI0 master data output (SPI serial output data from SMARC® module to the SPI device) | O 1.8V | PU 20k | |



Note

The conga-SA7 supports only the BIOS SPI flash memory on the SPI0 bus.

Table 20 eSPI/SPI1 Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|--------------|-------|---|----------|--------------|---------|
| ESPI_CK | P56 | ESPI master clock output. This pin provides the reference timing for all the serial input and output operations | O 1.8V | | |
| ESPI_CS0# | P54 | ESPI master chip select outputs. Driving Chip Select# low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Select# pin | O 1.8V | | |
| ESPI_CS1# | P55 | | | | |
| ESPI_IO_0 | P58 | ESPI master data input/outputs. These bi-directional input/output pins are used to transfer data between master and slaves. In single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO) | I/O 1.8V | | |
| ESPI_IO_1 | P57 | | | | |
| ESPI_IO_2 | S56 | | | | |
| ESPI_IO_3 | S57 | | | | |
| ESPI_RESET# | S58 | Resets the eSPI interface for both master and slaves. ESPI_RESET# is typically driven from eSPI master to eSPI slaves | O 1.8V | PD 75k | |
| ESPI_ALERT0# | S43 | This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for single master-single slave configuration where I/O[1] can be used to signal the alert event | I 1.8V | PU 100k 1.8V | |
| ESPI_ALERT1# | S44 | | | | |



Note

The conga-SA7 supports only general purpose devices on the eSPI/SPI1 bus.

Table 21 I2S Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|-------------|-------|--|----------|-------|---------------|
| I2S0_LRCK | S39 | Left and right audio synchronization clock | I/O 1.8V | | Not Supported |
| I2S0_SDOOUT | S40 | Digital audio output | O 1.8V | | |
| I2S0_SDIN | S41 | Digital audio input | I 1.8V | | |
| I2S0_CK | S42 | Digital audio clock | I/O 1.8V | | |
| AUDIO_MCK | S38 | Master clock output to audio codecs | O 1.8V | | |



Note

The conga-SA7 does not support I2S.

Table 22 HDA / I2S Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---------------------|-------|---------------------------------------|----------|--------|---------------------|
| HDA_SYNC | S50 | HD audio serial bus synchronization. | I/O 1.8V | | |
| HDA_SDO | S51 | HD audio serial data output to codec | O 1.8V | | |
| HDA_SDI | S52 | HD audio serial data input from codec | I 1.8V | | |
| HDA_CK | S53 | HD audio serial bit clock to codec | I/O 1.8V | PD 75k | |
| HDA_RST# / GPIO4 | P112 | HD audio codec reset | O 1.8V | PD 75k | HDA_RST# is default |

Table 23 I2C Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|------------|-------|----------------------------------|----------|--------|---------|
| I2C_GP_CK | S48 | I2C General purpose clock signal | I/O 1.8V | PU 2k2 | |
| I2C_GP_DAT | S49 | I2C General purpose data signal | I/O 1.8V | PU 2k2 | |

Table 24 Asynchronous Serial Port Signal Description

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|-----------|-------|---|--------|--------------|--------------------------------|
| SER0_TX | P129 | Asynchronous serial data output port 0 | O 1.8V | | congatec Board Controller UART |
| SER0_RX | P130 | Asynchronous serial data input port 0 | I 1.8V | | |
| SER0_RTS# | P131 | Request to Send handshake line for SER0 | O 1.8V | | |
| SER0_CTS# | P132 | Clear to Send handshake line for SER0 | I 1.8V | | |
| SER1_TX | P134 | Asynchronous serial data output port 1 | O 1.8V | | SoC UART |
| SER1_RX | P135 | Asynchronous serial data input port 1 | I 1.8V | PU 100k 1.8V | |
| SER2_TX | P136 | Asynchronous serial data output port 2 | O 1.8V | | |
| SER2_RX | P137 | Asynchronous serial data input port 2 | I 1.8V | PU 100k 1.8V | |
| SER2_RTS# | P138 | Request to Send handshake line for SER2 | O 1.8V | | |
| SER2_CTS# | P139 | Clear to Send handshake line for SER2 | I 1.8V | PU 100k 1.8V | |
| SER3_TX | P140 | Asynchronous serial data output port 3 | O 1.8V | | congatec Board Controller UART |
| SER3_RX | P141 | Asynchronous serial data input port 3 | I 1.8V | | |

Table 25 USB Pinout Description

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|--|--|---|-------------|--------|---------|
| USB0+ USB0- | P60 P61 | Differential USB 2.0 data pairs | I/O USB | | |
| USB1+ USB1- | P65 P66 | Differential USB 2.0 data pairs | I/O USB | | |
| USB2+ USB2- | P69 P70 | Differential USB 2.0 data pairs | I/O USB | | |
| USB3+ USB3- | S68 S69 | Differential USB 2.0 data pairs | I/O USB | | |
| USB4+ USB4- | S35 S36 | Differential USB 2.0 data pairs | I/O USB | | |
| USB5+ USB5- | S59 S60 | Differential USB 2.0 data pairs | I/O USB | | |
| USB0_EN_OC# USB1_EN_OC# USB2_EN_OC# USB3_EN_OC# USB4_EN_OC# USB5_EN_OC# | P62 P67 P71 P74 P76 S55 | Pulled low by module to disable USB0 power. Pulled low by carrier OD driver to indicate over-current situation. A pull-up to a 3.3V rail shall be present on the module | I/O OD 3.3V | PU 10k | |

| | | | | | |
|----------------------------|-------------|--|---------------|---------|---------------|
| USB0_VBUS_DET | P63 | USB host power detection when this port is used as a device | I USB VBUS 5V | PD 100k | Not supported |
| USB3_VBUS_DET | S37 | USB host power detection when this port is used as a device | I USB VBUS 5V | PD 100k | |
| USB0_OTG_ID USB3_OTG_ID | P64 S104 | USB OTG ID input, active high | I 3.3V | PU 100k | |
| USB2SSRX+ USB2SSRX- | S74 S75 | Receive signal differential pairs for SuperSpeed USB data coupling caps for RX pairs are off-module | I USB SS | | |
| USB2SSTX+ USB2SSTX- | S71 S72 | Transmit signal differential pairs for SuperSpeed USB data coupling caps for TX pairs are on-module | O USB SS | | |
| USB3SSRX+ USB3SSRX- | S65 S66 | Receive signal differential pairs for SuperSpeed USB data coupling caps for RX pairs are off-module | I USB SS | | |
| USB3SSTX+ USB3SSTX- | S62 S63 | Transmit signal differential pairs for SuperSpeed USB data coupling caps for TX pairs are on-module | O USB SS | | |



The conga-SA7 does not support USB OTG.

Table 26 PCIe Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|--------------------------------|------------|--|-------------|-------|---------------------------------|
| PCIE_A_TX+ PCIE_A_TX- | P89 P90 | Differential PCIe link A transmit data pair | O LVDS PCIe | | AC coupled with 220nF on module |
| PCIE_B_TX+ PCIE_B_TX- | S90 S91 | Differential PCIe link B transmit data pair | O LVDS PCIe | | AC coupled with 220nF on module |
| PCIE_C_TX+ PCIE_C_TX- | S81 S82 | Differential PCIe link C transmit data pair | O LVDS PCIe | | AC coupled with 220nF on module |
| PCIE_D_TX+ PCIE_D_TX- | S29 S30 | Differential PCIe link D transmit data pair | O LVDS PCIe | | AC coupled with 220nF on module |
| PCIE_A_RX+ PCIE_A_RX- | P86 P87 | Differential PCIe link A receive data pair | I LVDS PCIe | | |
| PCIE_B_RX+ PCIE_B_RX- | S87 S88 | Differential PCIe link B receive data pair | I LVDS PCIe | | |
| PCIE_C_RX+ PCIE_C_RX- | S78 S79 | Differential PCIe link C receive data pair | I LVDS PCIe | | |
| PCIE_D_RX+ PCIE_D_RX- | S32 S33 | Differential PCIe link D receive data pair | I LVDS PCIe | | |
| PCIE_A_REFCK+ PCIE_A_REFCK- | P83 P84 | Differential PCIe Link reference clock output DC coupled | O LVDS PCIe | | |

| | | | | | |
|--------------------------------|------------|--|-------------|--------|--|
| PCIE_B_REFCK+ PCIE_B_REFCK- | S84 S85 | Differential PCIe Link reference clock output DC coupled | O LVDS PCIe | | |
| PCIE_C_REFCK+ PCIE_C_REFCK- | P80 P81 | Differential PCIe Link reference clock output DC coupled | O LVDS PCIe | | |
| PCIE_A_RST# | P75 | PCIe port reset output | O 3.3V | | |
| PCIE_B_RST# | S76 | PCIe port reset output | O 3.3V | | |
| PCIE_C_RST# | S77 | PCIe port reset output | O 3.3V | | |
| PCIE_WAKE# | S146 | PCIe wake up interrupt to host common to PCIe links A, B, C, D | I OD 3.3V | PU 10k | |

Table 27 SERDES Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|------------------------------|------------|--|-------------|-------|---------------|
| SERDES_1_TX+ SERDES_1_TX- | S81 S82 | Differential SERDES 1 Transmit Data Pair | O PCIE | | Not supported |
| SERDES_1_RX+ SERDES_1_RX- | S78 S79 | Differential SERDES 1 Receive Data Pair | I PCIE | | |
| SERDES_0_TX+ SERDES_0_TX- | S29 S30 | Differential SERDES 0 Transmit Data Pair | O PCIE | | |
| SERDES_0_RX+ SERDES_0_RX- | S32 S33 | Differential SERDES 0 Receive Data Pair | I PCIE | | |
| MDIO_CLK | S45 | MDIO Signals to Configure Possible PHYs | O 1.8V | | |
| MDIO_DAT | S46 | MDIO Signals to Configure Possible PHYs | I/O OD 1.8V | | |



The conga-SA7 does not support SERDES.

Table 28 SATA Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|----------------------|------------|--|-----------|-------|---|
| SATA_TX+ SATA_TX- | P48 P49 | SATA 0 transmit differential data pair | O SATA | | Supports SATA specification, Revision 3.0 |
| SATA_RX+ SATA_RX- | P51 P52 | SATA 0 receive differential data pair | I SATA | | Supports SATA specification, Revision 3.0 |
| SATA_ACT# | S54 | Active low SATA activity indicator | O OD 3.3V | | Up to 24 mA LED current |

Table 29 Gigabit Ethernet Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|----------------------------------|------------|---|-------------|-------|--|
| GBE0_MDI0+ GBE0_MDI0- | P30 P29 | Bidirectional transmit/receive pair 0 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE1_MDI0+ GBE1_MDI0- | S17 S18 | Bidirectional transmit/receive pair 0 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE0_MDI1+ GBE0_MDI1- | P27 P26 | Bidirectional transmit/receive pair 1 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE1_MDI1+ GBE1_MDI1- | S20 S21 | Bidirectional transmit/receive pair 1 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE0_MDI2+ GBE0_MDI2- | P24 P23 | Bidirectional transmit/receive pair 2 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE1_MDI2+ GBE1_MDI2- | S23 S24 | Bidirectional transmit/receive pair 2 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE0_MDI3+ GBE0_MDI3- | P20 P19 | Bidirectional transmit/receive pair 3 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE1_MDI3+ GBE1_MDI3- | S26 S27 | Bidirectional transmit/receive pair 3 to magnetics (Media Dependent Interface) | I/O GBE MDI | | |
| GBE0_LINK100# GBE1_LINK100# | P21 S19 | Link speed indication LED for 100 Mb/s | O OD 3.3V | | Up to 24 mA LED current |
| GBE0_LINK1000# GBE1_LINK1000# | P22 S22 | Link speed indication LED for 1000 Mb/s | O OD 3.3V | | Up to 24 mA LED current |
| GBE0_LINK_ACT# GBE1_LINK_ACT# | P25 S31 | Link or activity indication LED. Driven low on link (10, 100 or 1000 Mb/s). Blinks on activity | O OD 3.3V | | Up to 24 mA LED current |
| GBE0_CTREF GBE1_CTREF | P28 S28 | Center-Tap reference voltage for carrier board Ethernet magnetic (if required by the module GBE PHY) | O | | Not connected |
| GBE0_SDP GBE1_SDP | P6 P5 | IEEE 1588 trigger signal. For hardware implementation of PTP (precision time protocol). This is typically implemented by the software-defined pins from the Ethernet controller. The SDP pins can be used for IEEE1588 auxiliary device connections and for other miscellaneous hardware or software-control purposes | I/O 3.3V | | Signals are provided by Intel Elkhart Lake SoC |

Table 30 Watchdog Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|---------------|------|-----------------------|--------|---------|----------------------------|
| WDT_TIME_OUT# | S145 | Watchdog timer output | O 1.8V | PD 100k | Driven only during runtime |

Table 31 GPIO Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|---------------------|------|--|----------|-------|---|
| GPIO0 | P108 | Bidirectional general purpose input/output | I/O 1.8V | | Controlled by the cBC. Default BIOS setting: General purpose output |
| GPIO1 | P109 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO2 | P110 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO3 | P111 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO4 / HDA_RST# | P112 | Bidirectional general purpose input/output Alternate use: HD audio reset HDA_RST# (active low output) | I/O 1.8V | | Controlled by the cBC. Default BIOS setting: HD audio reset |
| GPIO5 / PWM_OUT | P113 | Bidirectional general purpose input/output Alternate use: Pulse Width Modulation output PWM_OUT | I/O 1.8V | | Controlled by the cBC. Default BIOS setting: Pulse Width Modulation output |
| GPIO6 / TACHIN | P114 | Bidirectional general purpose input/output Alternate use: Tachometer input TACHIN | I/O 1.8V | | Controlled by the cBC. Default BIOS setting: Tachometer input |
| GPIO7 | P115 | Bidirectional general purpose input/output | I/O 1.8V | | Non-multiplexed GPIOs controlled by the cBC. Default BIOS setting: General purpose input |
| GPIO8 | P116 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO9 | P117 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO10 | P118 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO11 | P119 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO12 | S142 | Bidirectional general purpose input/output | I/O 1.8V | | |
| GPIO13 | S123 | Bidirectional general purpose input/output | I/O 1.8V | | |

 **Note**

Pins P112-P114 support alternate use by default. For GPIO functionality, change the default configuration in the BIOS menu under Advanced -> GPIO Configuration submenu.

Table 32 Management Pins Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|-------------------------|--------------|---|-------------|-----------------|----------------------|
| VIN_PWR_BAD# | S150 | Power bad indication from carrier board. Module and carrier power supplies (other than module and carrier power supervisory circuits) will not be enabled while this signal is held low by the carrier. Pulled up on module. Driven by OD part on carrier | I VDD_IN | PU 10k | |
| CARRIER_PWR_ON | S154 | Carrier board circuits (apart from power management and power path circuits) should not be powered up until the module asserts the CARRIER_PWR_ON signal. | O 1.8V | PD 100k | |
| CARRIER_STBY# | S153 | The module shall drive this signal low when the system is in a standby power state | O 1.8V | PD 100k | Connected to SUS_S3# |
| RESET_OUT# | P126 | General purpose reset output to carrier board | O 1.8V | PD 100k | |
| RESET_IN# | P127 | Reset input from carrier board. Carrier drives low to force a module reset, floats the line otherwise. Pulled up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k | |
| POWER_BTN# | P128 | Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k | |
| SLEEP# | S149 | Sleep indicator from carrier board. May be sourced from user Sleep button or carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k | |
| LID# | S148 | Lid open/close indication to module. Low indicates lid closure (which system may use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. Should be de-bounced on the module. Pulled-up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k | |
| BATLOW# | S156 | Battery low indication to module. Carrier to float the line in in-active state. Pulled up on module. Driven by OD part on carrier | I OD 1.8V | PU 10k | |
| I2C_PM_DAT I2C_PM_CK | P122 P121 | Power management I2C bus data and clock. On x86 systems these serve as SMB data and clock | I/O OD 1.8V | PU 2k2 | |
| CHARGING# | S151 | Held low by carrier during battery charging. Carrier to float the line when charge is complete. Pulled-up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k 3.3V | |
| CHARGER_PRSENT# | S152 | Held low by carrier if DC input for battery charger is present. Pulled up on module. Driven by OD part on carrier | I OD 3.3V | PU 10k 3.3V | |
| TEST# | S157 | Held low by carrier to invoke module vendor specific test function(s). Pulled up on module. Driven by OD part on carrier | I OD 3.3V | PU 100k 3.3V | |
| SMB_ALERT_1V8# | P1 | SM Bus Alert# (interrupt) signal | I OD 1.8V | PU 2k2 | |

Table 33 Boot Select Signal Description

| Signal Name | Pin | Description | I/O | PU/PD | Comment |
|--|----------------------|--|--------|--------|---------------|
| BOOT_SEL0# BOOT_SEL1# BOOT_SEL2# | P123 P124 P125 | Input straps determine the module boot device. Pulled up on module. Driven by OD part on carrier | I 1.8V | PU 10k | |
| FORCE_RECOV# | S155 | Low on this pin allows non-protected segments of module boot device to be rewritten or restored from an external USB Host on module USB0. The module USB0 operates in Client Mode when the Force Recovery function is invoked. Pulled high on the module. For SoCs that do not implement a USB based Force Recovery functions, then a low on the module FORCE_RECOV# pin may invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal may be used to load BIOS defaults. Pulled up on module. Driven by OD part on carrier | I 1.8V | PU 10k | Not supported |

Table 33.1 Boot Source Description

| Carrier Connection | | | Boot Source |
|--------------------|------------|------------|---|
| BOOT_SEL2# | BOOT_SEL1# | BOOT_SEL0# | |
| GND | GND | GND | Carrier SATA |
| GND | GND | Float | Carrier SD Card |
| GND | Float | GND | Carrier eSPI (CS0#) |
| GND | Float | Float | Carrier SPI (CS0#) |
| Float | GND | GND | Module device (NAND, NOR) - vendor specific |
| Float | GND | Float | Remote boot (GbE, serial) - vendor specific |
| Float | Float | GND | Module eMMC flash |
| Float | Float | Float | Module SPI |

 **Note**

1. The conga-SA7 supports only Carrier SPI boot source (GND, Float, Float) configuration.
2. For other boot source configurations, the conga-SA7 will boot from on-module SPI flash.

Table 33.2 Boot Strap Signal Description

| Signal | Pin # | Description of Boot Strap Signal | I/O | PU/PD | Comment |
|-----------------------|-------|---|----------|-----------|---------------|
| SPI0_DO | P46 | SPI0 master data output (SPI serial output data from SMARC® module to the SPI device) | O 1.8V | PU 20k | |
| HDA_SDO / I2S2_SDOOUT | S51 | HD audio serial data output to codec | O 1.8V | PD(i) 20k | |
| I2S0_CK | S42 | Digital audio clock | I/O 1.8V | PD(i) 20k | Not supported |
| I2S0_LRCK | S39 | Left and right audio synchronization clock | I/O 1.8V | PD(i) 20k | Not supported |



Caution

1. The signals listed in the table above are used as chipset configuration straps during system reset. In this condition (during reset), they are inputs that are pulled to the correct state by either SMARC internally implemented resistors or chipset internally implemented resistors that are located on the module.
2. No external DC loads or external pull-up or pull-down resistors should change the configuration of the signals listed in the above table.
3. External resistors may override the internal strap states and cause the SMARC module to malfunction and/or cause irreparable damage to the module.

Table 34 Power and GND Signal Descriptions

| Signal | Pin # | Description | I/O | PU/PD | Comment |
|---------|--|--|-----|-------|-------------------------|
| VDD_IN | P147, P148, P149, P150, P151, P152, P153, P154, P155, P156 | Module power input voltage—4.75V min. to 5.25V max. | P | | |
| GND | P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142 S3, S10, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158 | Power Ground | P | | |
| VDD_RTC | S147 | Low current RTC circuit backup power—3.0V nominal. May be sourced from a carrier based lithium cell or super cap. This option requires a customized variant. | P | | BOM option for sourcing |



Note

External 3.3 V is required for RTC battery implementation with supercap. Default conga-SA7 configuration does not support supercap charging. The supercap charging is only possible with a BOM option.

9 System Resources

9.1 I/O Address Assignment

The I/O address assignment of the conga-SA7 module is functionally identical with a standard PC/AT. The table below shows the most important addresses and the addresses that differ from the standard PC/AT configuration.

These Fixed address ranges are either positively decoded in the System Agent or subtractively routed to the Primary to Sideband Bridge (P2SB). The P2SB will claim many of the fixed I/O accesses and forward those transactions over sideband fabric to their functional target. Address ranges that are not listed or marked Reserved are NOT positively decoded by the PCH (unless assigned to one of the variable ranges) and will be internally terminated by the PCH.

On the conga-SA7 the Platform P2SB acts as the subtractive decoding agent. I/O Fix Addresses positively decoded by system Agents are listed on the following table.

Table 35 I/O Address Assignment

| I/O Address (hex) | Description |
|---------------------------|--|
| Interrupt Controller | 20h-21h, 24h-25h, 28h-29h, 2Ch-2Dh, 30h-31h, 34h-35h, 38h-39h, 3Ch-3Dh, A0h- A1h, A4h-A5h, A8h-A9h, ACh-ADh, B0h-B1h, B4h-B5h, B8h-B9h, Bch-BDh, 4D0h-4D1h |
| 8254 Timers | 40h-43h, 50h-53h |
| NMI Controller (CPU I/F) | 61h, 63h, 65h, 67h |
| Reset Generator (CPU I/F) | 92h |
| RTC | 70h-77h |
| Reset Generator (CPU) | CF9h |
| PMC | B2h-B3h |
| eSPI | 2Eh-2F, 4Eh-4Fh, 60h, 62h, 64h, 66h, 80h, 84h-86h, 8Ch-8Eh, 90h, 94h-96h, 98h, 9Ch-9Eh, 200-207h, 208-20Fh |

9.2 PCI Configuration Space Map

| Bus Number (hex) | Device Number (hex) | Function Number (hex) | Device ID | Description and Device ID |
|------------------|---------------------|-----------------------|-----------|--|
| 00h | 00h | 00h | 0x452E | Host Bridge |
| 00h | 02h | 00h | 0x4571 | Graphics and Display |
| 00h | 12h | 00h | 0x4B37 | Intel® Serial I/O: SPI Controller #2 |
| 00h | 14h | 00h | 0x4B7D | USB eXtensible Host Controller Interface (xHCI) |
| 00h | 14h | 01h | 0x4B7E | USB eXtensible Device Controller Interface (xDCI) ² |
| 00h | 14h | 02h | 0x4B7F | Memory Controller |
| 00h | 16h | 00h | 0x4B70 | Intel® Converged Security Engine (Intel® CSE) |
| 00h | 17h | 00h | 0x4B63 | SATA Controller (AHCI) |
| 00h | 18h | 00h | 0x4BC0 | Intel® Programmable Services Engine (Intel® PSE): I2C Controller #7 |
| 00h | 18h | 01h | 0x4BC1 | Intel® PSE: CAN Controller #0 ² |
| 00h | 18h | 02h | 0x4BC2 | Intel® PSE: CAN Controller #1 ² |
| 00h | 1Ah | 00h | 0x4B47 | embedded Multi Media Card (eMMC) Controller |
| 00h | 1Ah | 01h | 0x4B48 | Secure Digital (SD) & Secure Digital I/O Controller |
| 00h | 1Bh | 00h | 0x4BB9 | Intel® PSE: Inter-Integrated Circuit (I2C) Controller #0 |
| 00h | 1Ch | 00h | 0x4B38 | PCIe* Root Port #0 (PCIe 0, Single VC) ¹ |
| 00h | 1Ch | 01h | 0x4B39 | PCIe* Root Port #1 (PCIe 0, Single VC) ¹ |
| 00h | 1Ch | 02h | 0x4B3A | PCIe* Root Port #2 (PCIe 0, Single VC) ¹ |
| 00h | 1Ch | 03h | 0x4B3B | PCIe* Root Port #3 (PCIe 0, Single VC) ¹ |
| 00h | 1Ch | 04h | 0x4B3C | PCIe* Root Port #4 (PCIe 1, Multi VC) ¹ |
| 00h | 1Ch | 05h | 0x4B3D | PCIe* Root Port #5 (PCIe 2, Multi VC) ¹ |
| 00h | 1Ch | 06h | 0x4B3E | PCIe* Root Port #6 (PCIe 3, Multi VC) ¹ |
| 00h | 1Dh | 00h | 0x4BB3 | Intel® Programmable Services Engine (Intel® PSE): Local Host to PSE (LH2OSE) IPC |
| 00h | 1Dh | 01h | 0x4BA0 | Intel® PSE: Gigabit Ethernet Time Sensitive Networking (TSN) Controller #0 (RGMII: 1Gb Mode) |
| 00h | 1Dh | 02h | 0x4BB0 | Intel® PSE: Gigabit Ethernet Time Sensitive Networking (TSN) Controller #1 (RGMII: 1Gb Mode) |
| 00h | 1Eh | 00h | 0x4B28 | Intel® Serial I/O: UART Controller #0 ² |
| 00h | 1Eh | 01h | 0x4B28 | Intel Serial I/O: UART Controller #1 |
| 00h | 1Fh | 00h | 0x4B00 | Enhanced Serial Peripheral Interface (eSPI) Controller |
| 00h | 1Fh | 01h | 0x4B20 | Primary to Sideband Bridge (P2SB) |
| 00h | 1Fh | 02h | 0x4B21 | Power Management Controller (PMC) |

| | | | | |
|-----|-----|-----|--------|--|
| 00h | 1Fh | 04h | 0x4B23 | System Management Bus (SMBus) Controller |
| 00h | 1Fh | 05h | 0x4B24 | Serial Peripheral Interface (SPI) Controller for Flash & TPM |
| 00h | 1Fh | 07h | 0x4B26 | Intel® Trace Hub |



- Note**
1. To view these ports, attach a device to the corresponding PCI Express port or set the PCI Express port in the BIOS setup menu to “Enabled”.
 2. Disabled by default in the BIOS Setup menu.

9.3 I²C Bus and SMBus

System Management (SM) bus signals are connected to the Intel® chipset. The SM bus is not intended to be used by off-board non-system management devices. For more information about this subject, contact congatec technical support.

Table 36 Bus Accessibility

| Bus Type | Address | Device | Comment |
|-----------------|--|---------------------------|---|
| Primary I2C | 0x34 | I2S Codec | Only visible if it is present on conga-SEVAL carrier board |
| Primary I2C | 0xA0, 0xA2, 0xA4, 0xA6, 0xA8, 0xAA, 0xAC, 0xAE | EEPROM | Only visible if EEPROM is present on U40 of conga-SEVAL carrier board |
| Primary I2C | 0xE2 | Post Code Display | Only visible if Post Code is enabled on the conga-SEVAL carrier board |
| Primary SMBUS | 0x4E | TPS65981 | TPS65981 USB Type-C / PD controller U3 on conga-SEVAL carrier board |
| Primary SMBUS | 0xAE | PM I2C EEPROM | Only visible if EEPROM is present on U42 of conga-SEVAL carrier board |
| Primary SMBUS | 0xD6 | ICS9DBV0431 | Only visible in conga-SEVAL due to ICS9DBV0431 PCIe clock buffer U8 |
| Primary SMBUS | 0xF8, 0xFA, 0xFC, 0xFE | Reserved | Reserved addresses for future purposes according to SMBus Spec |
| Secondary SMBUS | 0xBC | SN56DP159 | SN56DP159 TMDS to HDMI level shifter re-timer |
| Secondary SMBUS | 0xC0 | LVDS Converter | Only Visible if LVDS Interface is enabled |
| Virtual I2C | 0x80, 0x90, 0xA0, 0xB0, 0xC0, 0xD0, 0xE0 | Intern BC Virtual Devices | |
| EPI | 0xA0-0xAE | EEPROM | Only Visible if an EEPROM is present on U28 of conga-SEVAL |



Address 16h is reserved for congatec Battery Management solutions.

10 BIOS Setup Description

10.1 Navigating the BIOS Setup Menu

The BIOS setup menu shows the features and options supported in the congatec BIOS. To access and navigate the BIOS setup menu, press the or <F2> key during POST. The right frame displays the key legend. Above the key legend is an area reserved for text messages. These text messages explain the options and the possible impacts when changing the selected option in the left frame.

10.2 BIOS Versions

The BIOS displays the BIOS project name and the revision code during POST, and on the main setup screen. The initial production BIOS for conga-SA7 is identified as SA70R1xx, where:

- R is the identifier for a BIOS ROM file,
- 1 is the so called feature number and
- xx is the major and minor revision number.

The SA70 binary size is 32 MB.

10.3 Updating the BIOS

BIOS updates are recommended to correct platform issues or enhance the feature set of the module. The conga-SA7 features a congatec/AMI AptioEFI firmware on an onboard flash ROM chip. You can update the firmware with the congatec System Utility. The utility has five versions—UEFI shell, DOS based command line¹, Win32 command line, Win32 GUI, and Linux version.

For more information about “Updating the BIOS” refer to the user’s guide for the congatec System Utility “CGUTLm1x.pdf” on the congatec website at www.congatec.com.



¹. *Deprecated*

10.3.1 Update from External Flash

For instructions on how to update the BIOS from external flash, refer to the AN7_External_BIOS_Update.pdf application note on the congatec website at <http://www.congatec.com>.

10.4 Supported Flash Devices

The conga-SA7 supports the following flash devices:

- W25R256JWXIQ


The flash device listed above can be used on the carrier board to support external BIOS.

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

Headquarters

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