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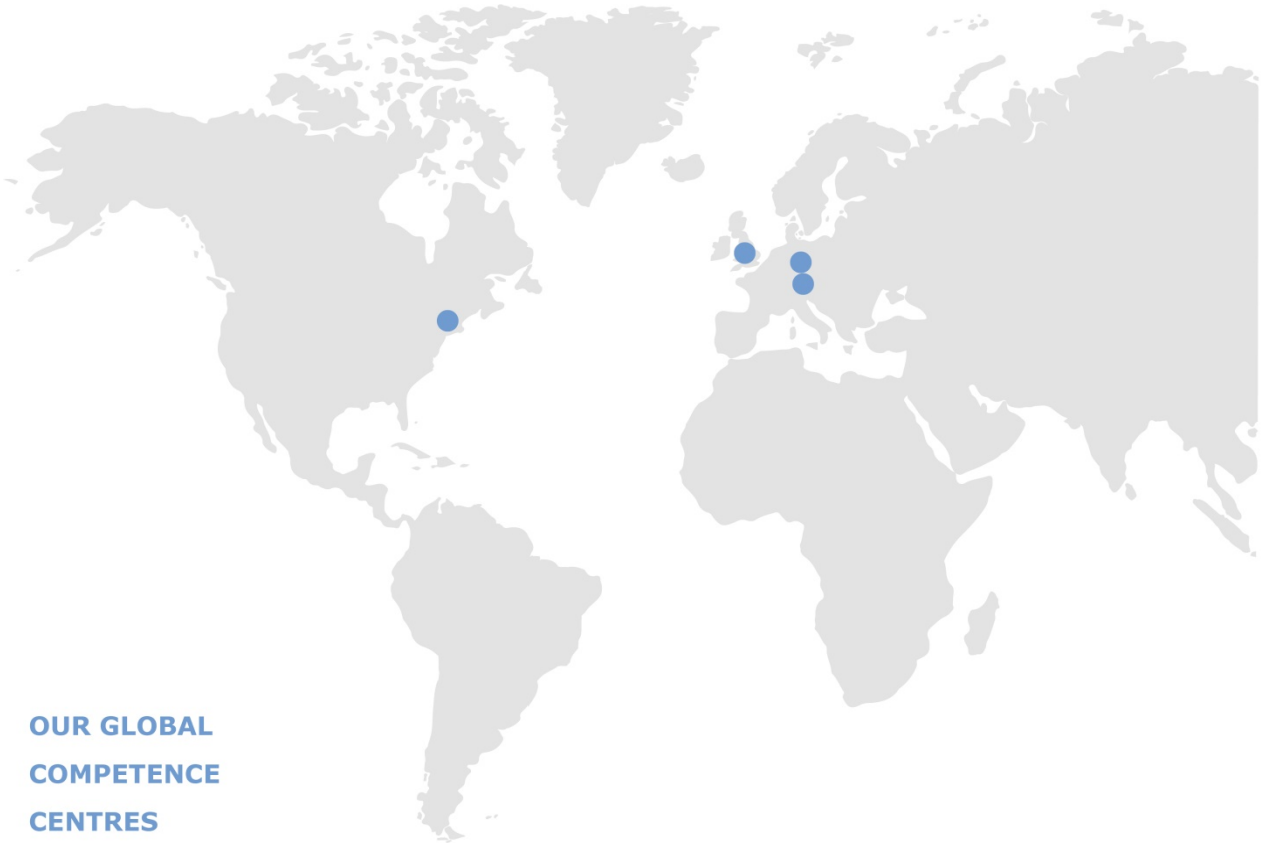

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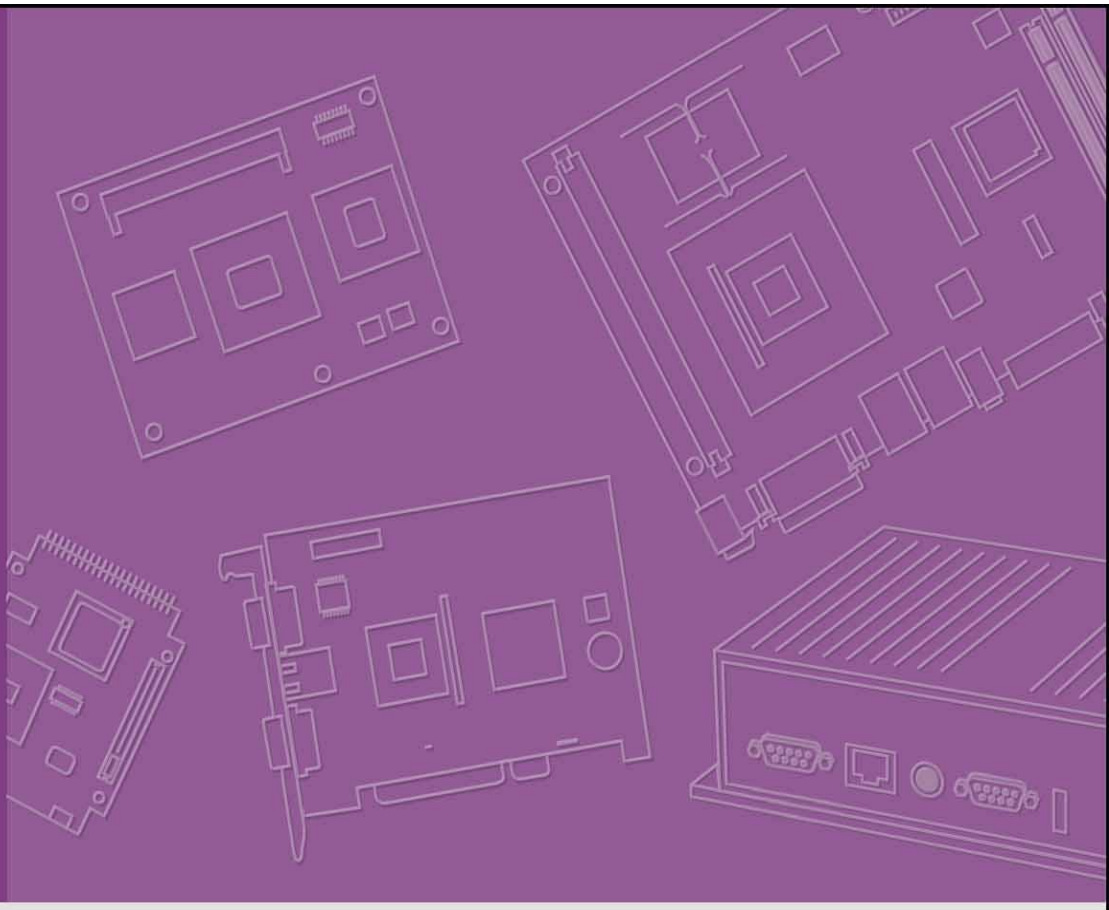

CarrierBoard Design Guide

SMARC

SOM-2532

R020 2020'09'29

ADVANTECH

Enabling an Intelligent Planet

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1 Introduction

1.1 About This Document

This document provides information for designing a custom system carrier board for SMARC modules. It includes Signal Descriptions, Routing Guidelines and Trace Length Guidelines. The main purpose is designing Carrier Board for helping customers fast and easy using the module of Advantech to be designed.

1.2 Signal Table Terminology

Table 1 below describes the terminology used in this section for the Signal Description tables.

The terms "Input" and "Output" and their abbreviations in Table 1 below refer to the Module's view, i.e. an input is an input for the Module and not for the Carrier-Board.

Table 1: Signal Direction and Type Definitions

Term	*Description*
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output
OD	Open drain
PU	PU (pull-up) resistor
PD	PD (pull-down) resistor
CMOS	Logic input or output
GBE MDI	Differential analog signaling for gigabit media dependent interface
DP	Low voltage differential signal for DisplayPort interface
D-PHY	Low voltage differential signal for MIPI CSI-2 cameras and DSI displays
M-PHY	Low voltage differential signal for MIPI CSI-3 cameras
LVDS	Low voltage differential signal for LCD displays
PCIE	Low voltage differential signal for PCIe
SATA	Low voltage differential signal for SATA
TMDS HDMI	Transition minimized differential signal for HDMI displays
USB	DC coupled differential signaling for traditional (non-Superspeed) USB signals
USB SS	Differential signal for SuperSpeed USB signals
USB VBUS 5V	5V tolerant input for USB VBUS detection
VDD_IN	Main power source from Carrier to Module
3.3V	3.3V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
1.8V	1.8V power domain: Active while CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)

3.3Vsb	3.3V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
1.8Vsb	1.8V standby power domain: Active while CARRIER_PWRON is high (regardless of CARRIER_SBY#)
Sleep	Module is in its lowest power state
Runtime	Module is full on. CARRIER_PWRON is high and CARRIER_SBY# is NOT active (i.e. both signals are high)
Standby	Module is in Standby State or higher

1.3 Terminology

Table 2: Conventions and Terminology

Terminology	*Description*
ADC	Analog to Digital Converter
ARM	Advanced RISC Machines
BCT	Boot Configuration Table
BSP	(software) Board Support Package
CAD	Computer Aided Design
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
CODEC	Coder – Decoder
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DB-9	Connector, D shaped, B shell size, 9 pins
DDC	Display Data Channel
DDI	Digital Display Interface
DE	Differential Ended (signal pair)
DNI	Do Not Install (component is not loaded)
DP	DisplayPort
DP++	Dual-mode DisplayPort
DSP	Digital Signal Processor
DSI	Display Serial Interface
EDID	Extended Display Identification Data
EEPROM	Electrically Erasable Programmable Read Only Memory
eMMC	Embedded Multi Media Card
ESD	Electro Static Discharge
FET	Field Effect Transistor
FIFO	First In First Out (buffer memory)

FS	Full Speed (USB 2.0 12 Mbps)
GBE	Gigabit Ethernet
Gbps	Gigabit per second
GPIO	General Purpose Input / Output
GPS	Global Positioning System
HAD	High Definition Audio – Intel defined format
HDMI	High Definition Multimedia Interface
HID	Human Interface Device: USB device class
HS	High Speed (USB 2.0 480 Mbps)
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Circuit – Sound
IEEE	Institute of Electrical and Electronics Engineers
IO	Input Output
ISO	International Organization for Standardization (French)
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
LED	Light Emitting Diode
Li-Ion	Lithium Ion (rechargeable battery technology)
LVDS	Low Voltage Differential Signaling
M2.5	Metric 2.5mm
M3	Metric 3.0mm
MAC	Media Access Controller (e.g. logic circuits in GBE)
Mbps	Megabit per second
MIPI	Mobile Industry Processor Interface
MLC	Multi Level Cell (flash memory reference)
MOD	Module (the SMARC Module) (schematic notation)
MO-297	Module Outline 297 (“Slim SATA” format)
MO-300	Module Outline 300 (mini-PCIe Express card format)
MPEG	Motion Picture Experts Group
MXM	Mobile pci eXpress Module
MXM3	MXM Revision 3
NAND	A high density flash memory technology
ns	Nano second (10 E -9)
NC	Not Connected
OS	Operating System
OTG	On the Go (USB term – device can be host or client)
PCB	Printed Circuit Board
PHY	Physical (transceiver) – drives cable

PICMG	PCI Industrial Computer Manufacturing Group
PCI	Peripheral Component Interface
PCIe	PCI Express
PCI-SIG	PCI Special Interest Group
PCM	Pulse-Code Modulation
PLL	Phase Locked Loop
POE	Power Over Ethernet
ps	Pico second (10 E -12)
PWM	Pulse Width Modulation
RGB	Video data in Red Green Blue pixel format
ROM	Read Only Memory
RS232	Recommend Standard 232 (asynchronous serial ports)
RS485	Asynchronous serial data, differential, multidrop
RTC	Real Time Clock (battery backed clock and memory)
SAR	Successive Approximation Register
SATA	Serial ATA (serial mass storage interface)
SD	Secure Digital (memory card)
SE	Single Ended (signal, as opposed to differential)
SGeT	Standardization Group for Embedded Technologies
SLC	Single Level Cell (flash memory reference)
SMARC	Smart Mobility Architecture
SMSC	A semiconductor company, now MICROCHIP
SOC	System On Chip
S/PDIF	Sony/Philips Digital Interconnect Format
SPI	Serial Peripheral Interface
SSD	Solid State Disk
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver Transmitter
UL	Underwriters Laboratories
USB	Universal Serial Bus
VESA	Video Electronics Standards Association
WEC7	Windows Embedded Compact 7 (an OS)
YUV	Video data format, more common in television
X5R	Ceramic capacitor dielectric – good quality
X7R	Ceramic capacitor dielectric – best quality
X86	Intel architecture (80x86) CPUs

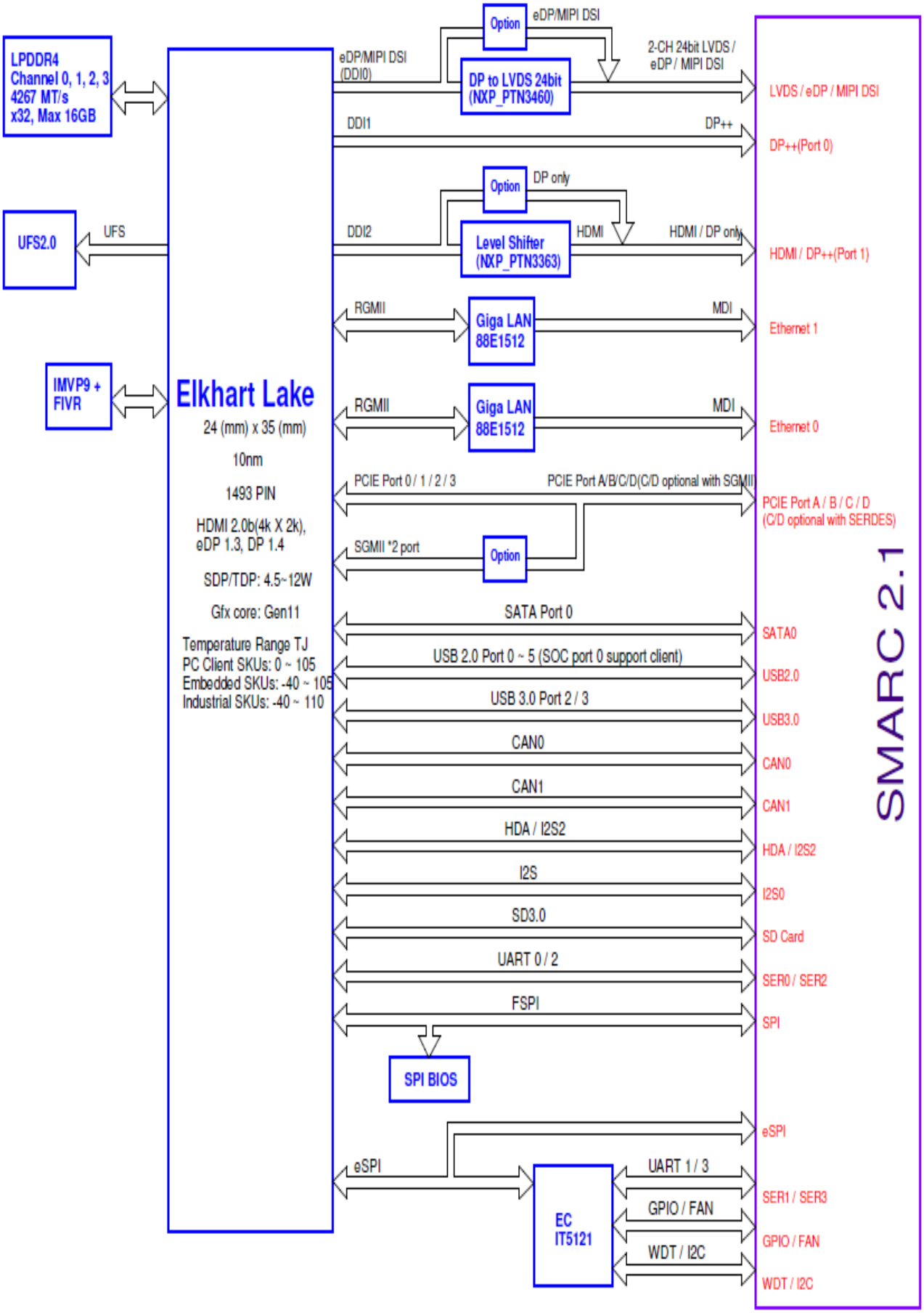
1.4 Reference Documents

Document
SMACR Design Guide 2.0 March 23, 2017
SMACR Hardware Specification 2.11 May 20, 2020
Intel EDS Document
Intel Layout Guide Document
ATX12V Power Supply Design Guide Rev. 2.01

1.5 Revision History

Revision	Date	PCB Rev.	Changes
0.10	09 06, 2020	A101-1	SOM-2532 design for SMARC R2.1
0.20	09 29, 2020	A101-1	SOM-2532 design for SMARC R2.11

1.6 SOM-2532 Block Diagram



2 SMARC Interfaces

2.1 SMARC 2.11 Connector Pin-out

Table 3: SMARC 2.11 Pin-out

Connector

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P1	SMB_ALERT		S1	CSI1_TX+ / I2C_CAM1_CK	NC
P2	GND		S2	CSI1_TX- / I2C_CAM1_DAT	NC
P3	CSI1_CK+	NC	S3	GND	
P4	CSI1_CK-	NC	S4	RSVD	
P5	GBE1_SDP	NC	S5	CSI0_TX+ / I2C_CAM0_CK	NC
P6	GBE0_SDP	NC	S6	CAM_MCK	NC
P7	CSI1_RX0+	NC	S7	CSI0_TX- / I2C_CAM0_DAT	NC
P8	CSI1_RX0-	NC	S8	CSI0_CK+	NC
P9	GND		S9	CSI0_CK-	NC
P10	CSI1_RX1+	NC	S10	GND	
P11	CSI1_RX1-	NC	S11	CSI0_RX0+	NC
P12	GND		S12	CSI0_RX0-	NC
P13	CSI1_RX2+	NC	S13	GND	
P14	CSI1_RX2-	NC	S14	CSI0_RX1+	NC
P15	GND		S15	CSI0_RX1-	NC
P16	CSI1_RX3+	NC	S16	GND	
P17	CSI1_RX3-	NC	S17	GBE1_MDI0+	
P18	GND		S18	GBE1_MDI0-	
P19	GBE0_MDI3-		S19	GBE1_LINK100#	
P20	GBE0_MDI3+		S20	GBE1_MDI1+	
P21	GBE0_LINK100#		S21	GBE1_MDI1-	
P22	GBE0_LINK1000#		S22	GBE1_LINK1000#	
P23	GBE0_MDI2-		S23	GBE1_MDI2+	
P24	GBE0_MDI2+		S24	GBE1_MDI2-	
P25	GBE0_LINK_ACT#		S25	GND	
P26	GBE0_MDI1-		S26	GBE1_MDI3+	
P27	GBE0_MDI1+		S27	GBE1_MDI3-	
P28	GBE0_CTREF	NC	S28	GBE1_CTREF	NC
P29	GBE0_MDI0-		S29	PCIE_D_TX+ / SERDES_0_TX+	SEDRES is option function
P30	GBE0_MDI0+		S30	PCIE_D_TX- / SERDES_0_TX-	SEDRES is option function
P31	SPI0_CS1#		S31	GBE1_LINK_ACT#	
P32	GND		S32	PCIE_D_RX+ / SERDES_0_RX+	SEDRES is option function
P33	SDIO_WP		S33	PCIE_D_RX- / SERDES_0_RX-	SEDRES is option function
P34	SDIO_CMD		S34	GND	
P35	SDIO_CD#		S35	USB4+	
P36	SDIO_CK		S36	USB4-	

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P37	SDIO_PWR_EN		S37	USB3_VBUS_DET	NC
P38	GND		S38	AUDIO_MCK	
P39	SDIO_D0		S39	I2S0_LRCK	
P40	SDIO_D1		S40	I2S0_SDOUT	
P41	SDIO_D2		S41	I2S0_SDIN	
P42	SDIO_D3		S42	I2S0_CK	
P43	SPI0_CS0#		S43	ESPI_ALERT0#	
P44	SPI0_CK		S44	ESPI_ALERT1#	
P45	SPI0_DIN		S45	MDIO_CLK	
P46	SPI0_DO		S46	MDIO_DAT	
P47	GND		S47	GND	
P48	SATA_TX+		S48	I2C_GP_CK	Default from EC, Chipset is option function
P49	SATA_TX-		S49	I2C_GP_DAT	Default from EC, Chipset is option function
P50	GND		S50	HDA_SYNC / I2S2_LRCK	HDA Only
P51	SATA_RX+		S51	HDA_SDO / I2S2_SDOUT	HDA Only
P52	SATA_RX-		S52	HDA_SDI / I2S2_SDIN	HDA Only
P53	GND		S53	HDA_CK / I2S2_CK	HDA Only
P54	ESPI_CS0# / SPI1_CS0# / QSPI_CS0#	ESPI Only	S54	SATA_ACT#	
P55	ESPI_CS1# / SPI1_CS1# / QSPI_CS1#	ESPI Only	S55	USB5_EN_OC#	
P56	ESPI_CK / SPI1_ CK / QSPI_CK	ESPI Only	S56	ESPI_IO_2 / QSPI_IO_2	ESPI Only
P57	ESPI_IO_1 / SPI1_DIN / QSPI_IO_1	ESPI Only	S57	ESPI_IO_3 / QSPI_IO_3	ESPI Only
P58	ESPI_IO_0 / SPI1_DO /QSPI_IO_0	ESPI Only	S58	ESPI_RESET#	
P59	GND		S59	USB5+	
P60	USB0+		S60	USB5-	
P61	USB0-		S61	GND	
P62	USB0_EN_OC#		S62	USB3_SSTX+	
P63	USB0_VBUS_DET		S63	USB3_SSTX-	
P64	USB0_OTG_ID		S64	GND	
P65	USB1+		S65	USB3_SSRX+	
P66	USB1-		S66	USB3_SSRX-	
P67	USB1_EN_OC#		S67	GND	
P68	GND		S68	USB3+	
P69	USB2+		S69	USB3-	

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P70	USB2-		S70	GND	
P71	USB2_EN_OC#		S71	USB2_SSTX+	
P72	RSVD		S72	USB2_SSTX-	
P73	RSVD		S73	GND	
P74	USB3_EN_OC#		S74	USB2_SSRX+	
P75	PCIE_A_RST#		S75	USB2_SSRX-	
P76	USB4_EN_OC#		S76	PCIE_B_RST#	
P77	PCIE_B_CKREQ#		S77	PCIE_C_RST#	
P78	PCIE_A_CKREQ#		S78	PCIE_C_RX+ / SERDES_1_RX+	SEDRES is option function
P79	GND		S79	PCIE_C_RX- / SERDES_1_RX-	SEDRES is option function
P80	PCIE_C_REFCK+		S80	GND	
P81	PCIE_C_REFCK-		S81	PCIE_C_TX+ / SERDES_1_TX+	SEDRES is option function
P82	GND		S82	PCIE_C_TX- / SERDES_1_TX-	SEDRES is option function
P83	PCIE_A_REFCK+		S83	GND	
P84	PCIE_A_REFCK-		S84	PCIE_B_REFCK+	
P85	GND		S85	PCIE_B_REFCK-	
P86	PCIE_A_RX+		S86	GND	
P87	PCIE_A_RX-		S87	PCIE_B_RX+	
P88	GND		S88	PCIE_B_RX-	
P89	PCIE_A_TX+		S89	GND	
P90	PCIE_A_TX-		S90	PCIE_B_TX+	
P91	GND		S91	PCIE_B_TX-	
P92	HDMI_D2+ / DP1_LANE0+	DP is option function	S92	GND	
P93	HDMI_D2- / DP1_LANE0-	DP is option function	S93	DP0_LANE0+	
P94	GND		S94	DP0_LANE0-	
P95	HDMI_D1+ / DP1_LANE1+	DP is option function	S95	DP0_AUX_SEL	
P96	HDMI_D1- / DP1_LANE1-	DP is option function	S96	DP0_LANE1+	
P97	GND		S97	DP0_LANE1-	
P98	HDMI_D0+ / DP1_LANE2+	DP is option function	S98	DP0_HPD	
P99	HDMI_D0- / DP1_LANE2-	DP is option function	S99	DP0_LANE2+	
P100	GND		S100	DP0_LANE2-	

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P101	HDMI_CK+ / DP1_LANE3+	DP is option function	S101	GND	
P102	HDMI_CK- / DP1_LANE3-	DP is option function	S102	DP0_LANE3+	
P103	GND		S103	DP0_LANE3-	
P104	HDMI_HPD / DP1_HPD	DP is option function	S104	USB3_OTG_ID	NC
P105	HDMI_CTRL_CK / DP1_AUX+	DP is option function	S105	DP0_AUX+	
P106	HDMI_CTRL_DAT / DP1_AUX-	DP is option function	S106	DP0_AUX-	
P107	DP1_AUX_SEL		S107	LCD1_BKLT_EN	
P108	GPIO0 / CAM0_PWR#	GPIO Only	S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P109	GPIO1 / CAM1_PWR#	GPIO Only	S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P110	GPIO2 / CAM0_RST#	GPIO Only	S110	GND	
P111	GPIO3 / CAM1_RST#	GPIO Only	S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P112	GPIO4 / HDA_RST#	HDA_RST#	S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P113	GPIO5 / PWM_OUT	Default PWM_OUT, GPIO5 is option function.	S113	eDP1_HPD / DSI1_TE	NC
P114	GPIO6 / TACHIN	Default TACHIN, GPIO6 is option function	S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P115	GPIO7		S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P116	GPIO8		S116	LCD1_VDD_EN	
P117	GPIO9		S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P118	GPIO10		S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P119	GPIO11		S119	GND	
P120	GND		S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function..
P121	I2C_PM_CK		S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS Only If eDP0 or DSI0 function is used, this pin will be no function.
P122	I2C_PM_DAT		S122	LCD1_BKLT_PWM	
P123	BOOT_SEL0#	NC	S123	GPIO13	
P124	BOOT_SEL1#	NC	S124	GND	
P125	BOOT_SEL2#		S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	Default LVDS, eDP or DSI are option functions
P126	RESET_OUT#		S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	Default LVDS, eDP or DSI are option functions
P127	RESET_IN#		S127	LCD0_BKLT_EN	
P128	POWER_BTN#		S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	Default LVDS, eDP or DSI are option functions
P129	SER0_TX		S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	Default LVDS, eDP or DSI are option functions
P130	SER0_RX		S130	GND	
P131	SER0_RTS#		S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	Default LVDS, eDP or DSI are option functions
P132	SER0_CTS#		S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	Default LVDS, eDP or DSI are option functions
P133	GND		S133	LCD0_VDD_EN	
P134	SER1_TX		S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	Default LVDS, eDP or DSI are option functions
P135	SER1_RX		S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	Default LVDS, eDP or DSI are option functions

Pin#	Description	SOM-2532 Difference	Pin#	Description	SOM-2532 Difference
P136	SER2_TX		S136	GND	
P137	SER2_RX		S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	Default LVDS, eDP or DSI are option functions
P138	SER2_RTS#		S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	Default LVDS, eDP or DSI are option functions
P139	SER2_CTS#		S139	I2C_LCD_CK	LVDS DDC CLK
P140	SER3_TX		S140	I2C_LCD_DAT	LVDS DDC DAT
P141	SER3_RX		S141	LCD0_BKLT_PWM	
P142	GND		S142	GPIO12	
P143	CAN0_TX		S143	GND	
P144	CAN0_RX		S144	eDP0_HPD / DSI0_TE	
P145	CAN1_TX		S145	WDT_TIME_OUT#	
P146	CAN1_RX		S146	PCIE_WAKE#	
P147	VDD_IN		S147	VDD_RTC	
P148	VDD_IN		S148	LID#	
P149	VDD_IN		S149	SLEEP#	
P150	VDD_IN		S150	VIN_PWR_BAD#	
P151	VDD_IN		S151	CHARGING#	
P152	VDD_IN		S152	CHARGER_PRSNT#	
P153	VDD_IN		S153	CARRIER_STBY#	
P154	VDD_IN		S154	CARRIER_PWR_ON	
P155	VDD_IN		S155	FORCE_RECOV#	
P156	VDD_IN		S156	BATLOW#	
			S157	TEST#	
			S158	GND	

2.2 PCI Express

2.2.1 PCIe Groups

The Module *may* implement up to four PCIe lanes. The links *may* be PCIe Gen 1, 2 or 3, as the Module chip or chipset allows.

The Module PCIe links are primarily PCIe Root Complexes. If the chipset allows it, the PCIe link(s) *may* alternatively be configured as a PCIe target(s). This is Advantech specific.

Modules should implement the PCIe Link A port. Modules may implement the PCIe Links B, C and D ports. Fill order is A, B, C then D.

PCIe lanes C and D may implement SERDES alternatively.

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. SMARC currently calls out x1, x2 and x4 operation. Up to four PCIe x1 links may be implemented on a SMARC Module. There are three generations of PCIe defined, with each successive generation offering a speed increase, per the table below. The PCIe generation that may be supported on a particular SMARC Module is design and SOC dependent.

Table 4: PCIe Data Transfer Rates

PCIe Generation	Link Speed (x1 link)	Encoding / Overhead	Net Data Transfer Rate
1	2.5 GT/s	8b/10b 20%	250 MB/s
2	5.0 GT/s	8b/10b 20%	500 MB/s
3	8.0 GT/s	128b / 130b 1.54%	985 MB/s

PCI Express is defined in a series of documents maintained by the PCI Special Interest Group (www.pci-sig.org). The three most important documents to obtain are the Base Specification, the Card Electromechanical (CEM) Specification (which describes slot cards) and the Mini Card Electromechanical Specification (which describes the small format cards commonly referred to as Mini-PCIe cards).

2.2.2 PCI Express Link Width

A connection between any two PCIe devices is known as a link, and is built up from a collection of one or more lanes. All devices ***shall*** support at least one single lane (x1) link. Devices may optionally support wider links composed of 2 or 4 lanes. Therefore the root complex ***may*** support different link width additionally to the x1 configuration.

The SMARC specification allows for multiple PCI Express link configurations. Check with Advantech which configurations are supported.

SMARC 2.11 adds CKREQ# signals for PCIe A and B to allow for enhanced power saving. The clock for PCIe D should be generated from the fixed clock of PCIe C.

Table 5: PCI Express Link Width

<table>
<tr><td>SMARC PCIe Lane</td><td colspan="5">Possible Link Configuration</td></tr>
<tr><td>PCIe A</td><td>x1</td><td>x1</td><td rowspan="2">x2</td><td rowspan="2">x2</td><td rowspan="4">x4</td></tr>
<tr><td>PCIe B</td><td>x1</td><td>x1</td></tr>
<tr><td>PCIe C</td><td>x1</td><td rowspan="2">x2</td><td>x1</td><td rowspan="2">x2</td></tr>
<tr><td>PCIe D</td><td>x1</td><td>x1</td></tr>
<tr><td>SMARC PCIe Lane</td><td colspan="5">REFCK and RST Assignments</td></tr>
<tr><td>PCIe A</td><td>PCIE_A_REFCK
PCIE_A_CKREQ#
PCIE_A_RST#</td><td>PCIE_A_REFCK
PCIE_A_CKREQ#
PCIE_A_RST#</td><td rowspan="2">PCIE_A_REFCK
PCIE_A_CKREQ#
PCIE_A_RST#</td><td rowspan="2">PCIE_A_REFCK
PCIE_A_CKREQ#
PCIE_A_RST#</td><td rowspan="4">PCIE_A_REFCK
PCIE_A_CKREQ#
PCIE_A_RST#</td></tr>
<tr><td>PCIe B</td><td>PCIE_B_REFCK
PCIE_B_CKREQ#
PCIE_B_RST#</td><td>PCIE_B_REFCK
PCIE_B_CKREQ#
PCIE_B_RST#</td></tr>
<tr><td>PCIe C</td><td>PCIE_C_REFCK
PCIE_C_RST#</td><td rowspan="2">PCIE_C_REFCK
PCIE_C_RST#</td><td>PCIE_B_REFCK
PCIE_B_CKREQ#
PCIE_B_RST#</td><td rowspan="2">PCIE_B_REFCK
PCIE_B_CKREQ#
PCIE_B_RST#</td></tr>
<tr><td>PCIe D</td><td>to be generated via buffer from PCIe C signals</td><td>PCIE_C_REFCK
PCIE_C_RST#</td></tr>
</table>

2.2.3 General Purpose PCIe Signal Definitions

Table 6: General Purpose PCI Express Signal Descriptions

Signal	Pin#	Description	I/O	Note
PCIE_A_RX+ PCIE_A_RX-	P86 P87	PCIe channel A. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near SMARC to PCIEA x1 device PETpA. Slot - Connect to PCIEA x1 Conn pin A16, A17 PERpA. N/C if not used.	I PCIE Runtime	
PCIE_A_TX+ PCIE_A_TX-	P89 P90	PCIe channel A. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIEA x1 device PERpA. Slot - Connect to PCIEA x1 Conn pin B14, B15 PETpA. N/C if not used	O PCIE Runtime	
PCIE_A_REFCK+ PCIE_A_REFCK-	P83 P84	PCIe Reference Clock for PCIe lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE Runtime	
PCIE_A_RST#	P75	Reset output from Module to Carrier Board. Active low. Module has integrated 3.3V buffer and series resistor. Connect to reset pin of devices except PCI slots or devices. N/C if not used.	O CMOS Runtime 3.3V	
PCIE_A_CKREQ#	P78	PCIe Port A clock request. Can be used for power saving mode on PCIe - Pulled up or terminated on Module. N/C if not used.	IO OD CMOS Runtime 3.3V	

Signal	Pin#	Description	I/O	Note
PCIE_B_RX+ PCIE_B_RX-	S87 S88	PCIe channel B. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near SMARC to PCIEB x1 device PETpB. Slot - Connect to PCIEB x1 Conn pin A16, A17 PERpB. N/C if not used.	I PCIE Runtime	
PCIE_B_TX+ PCIE_B_TX-	S90 S91	PCIe channel A. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIEB x1 device PERpB. Slot - Connect to PCIEB x1 Conn pin B14, B15 PETpB. N/C if not used	O PCIE Runtime	
PCIE_B_REFCK+ PCIE_B_REFCK-	S84 S85	PCIe Reference Clock for PCIe lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE Runtime	
PCIE_B_RST#	S76	Reset output from Module to Carrier Board. Active low. Module has integrated 3.3V buffer and series resistor. Connect to reset pin of devices except PCI slots or devices. N/C if not used.	O CMOS Runtime 3.3V	
PCIE_B_CKREQ#	P77	PCIe Port A clock request. Can be used for power saving mode on PCIe - Pulled up or terminated on Module. N/C if not used.	IO OD CMOS Runtime 3.3V	
PCIE_C_RX+ / SERDES_1_RX+ PCIE_C_RX- / SERDES_1_RX-	S78 S79	PCIe channel C. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1uF near SMARC to PCIEC x1 device PETpC. Slot - Connect to PCIEC x1 Conn pin A16, A17 PERpC. N/C if not used.	I PCIE Runtime	

Signal	Pin#	Description	I/O	Note
PCIE_C_TX+ / SERDES_1_TX+ PCIE_C_TX- / SERDES_1_TX-	S81 S82	PCIe channel C. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIEC x1 device PERpC. Slot - Connect to PCIEC x1 Conn pin B14, B15 PETpC. N/C if not used	O PCIE Runtime	
PCIE_C_REFCK+ PCIE_C_REFCK-	P80 P81	PCIe Reference Clock for PCIe lanes. Carrier Board: Connect 0Ω in series to Device - PCIE device REFCLK+, REFCLK-. Slot - PCIE Conn pin A13 REFCLK+, A14 REFCLK-. *Connect to PCIE Clock Buffer input to provide PCIE clocks output for more than one PCIE devices or slots. N/C if not used.	O PCIE Runtime	
PCIE_C_RST#	S77	Reset output from Module to Carrier Board. Active low. Module has integrated 3.3V buffer and series resistor. Connect to reset pin of devices except PCI slots or devices. N/C if not used.	O CMOS Runtime 3.3V	
PCIE_D_RX+ / SERDES_0_RX+ PCIE_D_RX- / SERDES_0_RX-	S32 S33	PCIe channel D. Receive Input differential pair. Carrier Board: Device - Connect AC Coupling cap 0.1/0.22uF near SMARC to PCIED x1 device PETpD. Slot - Connect to PCIED x1 Conn pin A16, A17 PERpD. N/C if not used.	I PCIE Runtime	1
PCIE_D_TX+ / SERDES_0_TX+ PCIE_D_TX- / SERDES_0_TX-	S29 S30	PCIe channel C. Transmit Output differential pair. Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to PCIED x1 device PERpD. Slot - Connect to PCIED x1 Conn pin B14, B15 PETpD. N/C if not used	O PCIE Runtime	1

Signal	Pin#	Description	I/O	Note
PCIE_WAKE#	S146	PCIe wake up interrupt to host – common to PCIe links A, B, C, D – pulled up or terminated on Module This signal has 10K Ω pull up to 3.3V_DUAL on the module. Device - Connect to WAKE# pin of PCIE device. Slot - Connect to WAKE# pin B11 of PCIE slot. Express Card - Connect to WAKE# pin 11 of Express Card socket. N/C if not used.	I OD CMOS Standby 3.3V	

Note

1. SEDRES is option function.

2.2.4 PCI Express* General Routing Guidelines

2.2.4.1 PCI Express Differential Transitional Via Recommendations

Transitional vias will use oval-shapes anti-pads on all plane layers. This can be created using a rectangular-shaped void to overlap with the usual round-shaped via anti-pad. The vias must also have a symmetrical trace entry.

Figure 2 and Table 7 provides the transitional differential via pad stack details.

Figure 1: Differential Transitional Via Layout

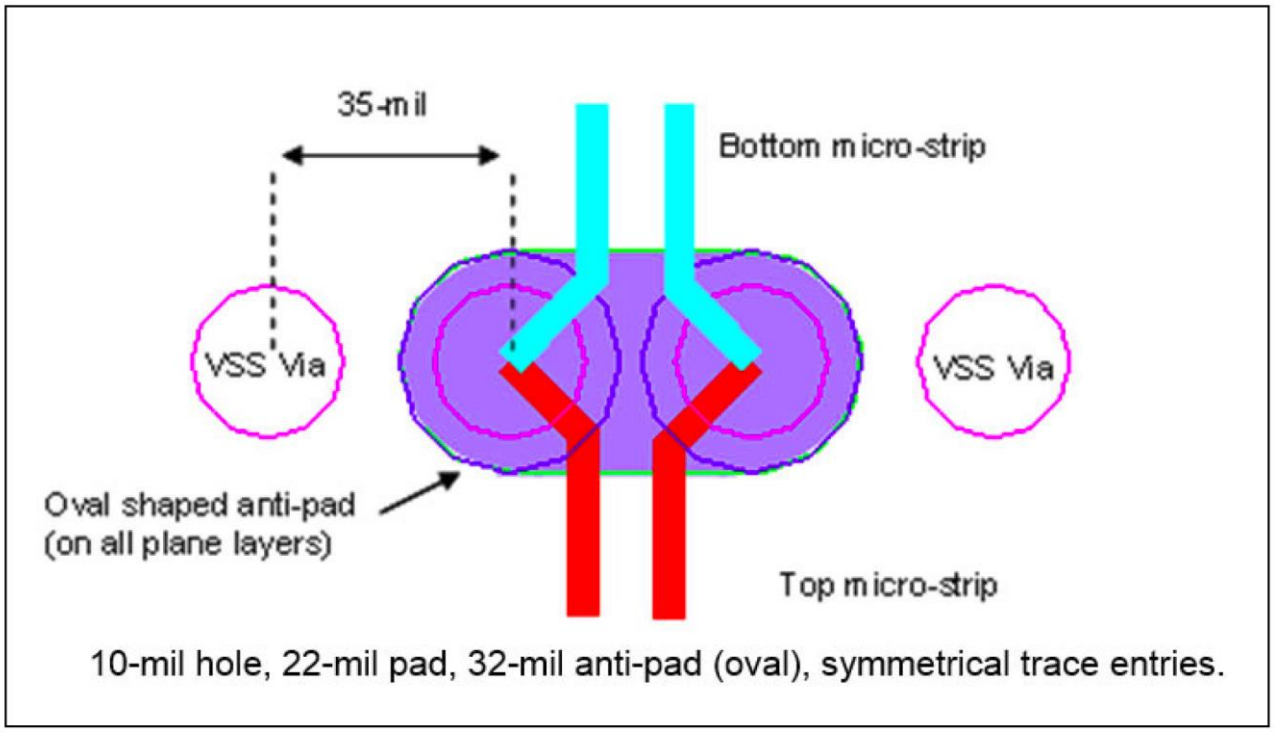


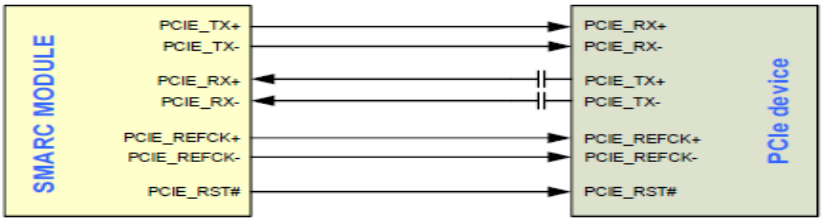
Table 7: Differential Transitional Via Layout Recommendations

Parameter	Units	Recommendation
Via Diameter	mils	10
Via Pad Size	mils	22
Oval-Shaped Anti-Pad Size	mils	32
Via to via Distance(centered)	mils	35

2.2.4.2 PCIe x1 Device Down on Carrier

An example of a PCIe x1 “device down” on the Carrier is shown below. Coupling caps on the SMARC PCIe TX and PCIe reference clock pairs are not needed on the Carrier. Coupling caps on the SMARC PCIe RX pair (TX pair from the Carrier PCIe device) are needed. They should be placed close to the Carrier device PCIe TX pins. Use 0402 package 0.2 or 0.1 uF X7R or X5R dielectric discrete ceramic capacitors. Do not use a capacitor array. Place the parts in a way to preserve the symmetry of the differential pair. Usually they are placed close to the Carrier device TX pins to avoid a via transition

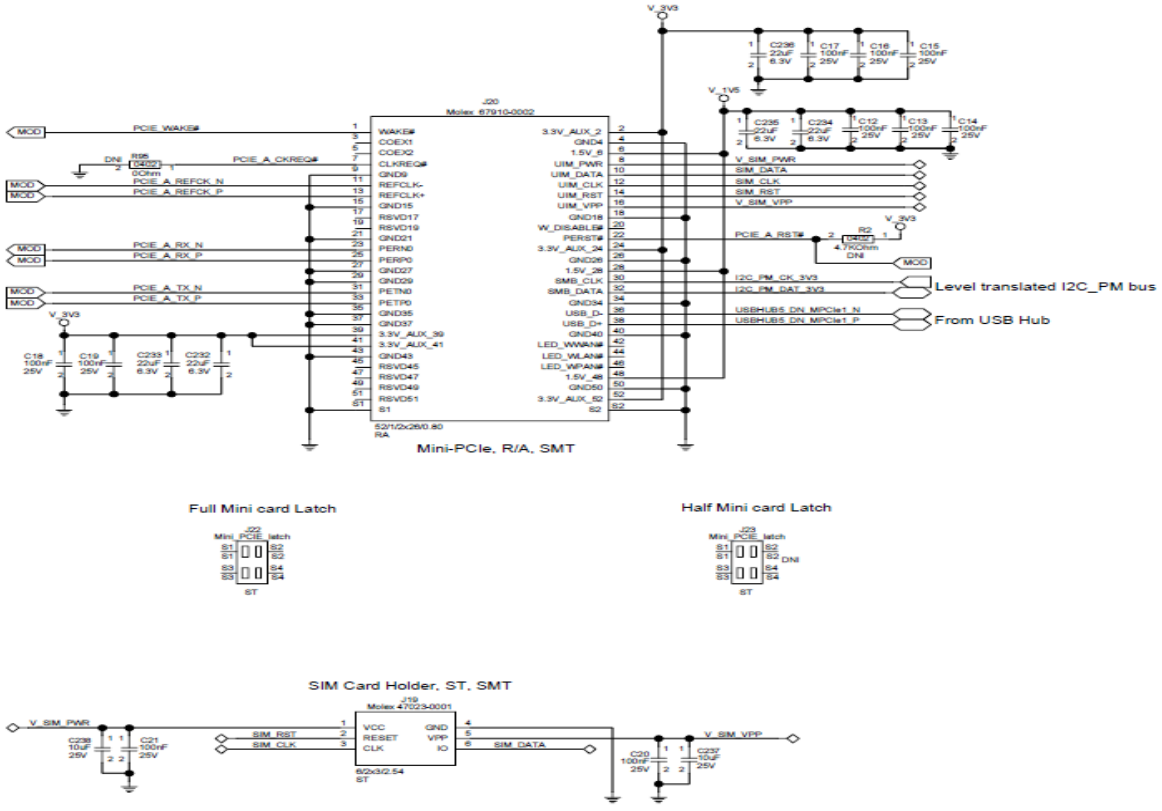
Figure 2: Interfacing a PCIe x1 Carrier Board Device



2.2.4.3 Mini-PCIe Slot

A SMARC Mini-PCIe implementation example is shown below. Mini-PCIe cards are defined to have pins for PCIe x1 and also a USB interface. A given card generally uses only one or the other. If you know exactly what Mini-PCIe card you plan to use, it is possible to omit either USB or PCIe. Generally, Mini-PCIe 802.11 WiFi cards use the PCIe interface and cellular modem cards use the USB interface.

Figure 3: Mini-PCIe Slot



2.2.5 PCI Express* Trace Length Guidelines

Figure 4: Topology for PCI Express Slot Card.

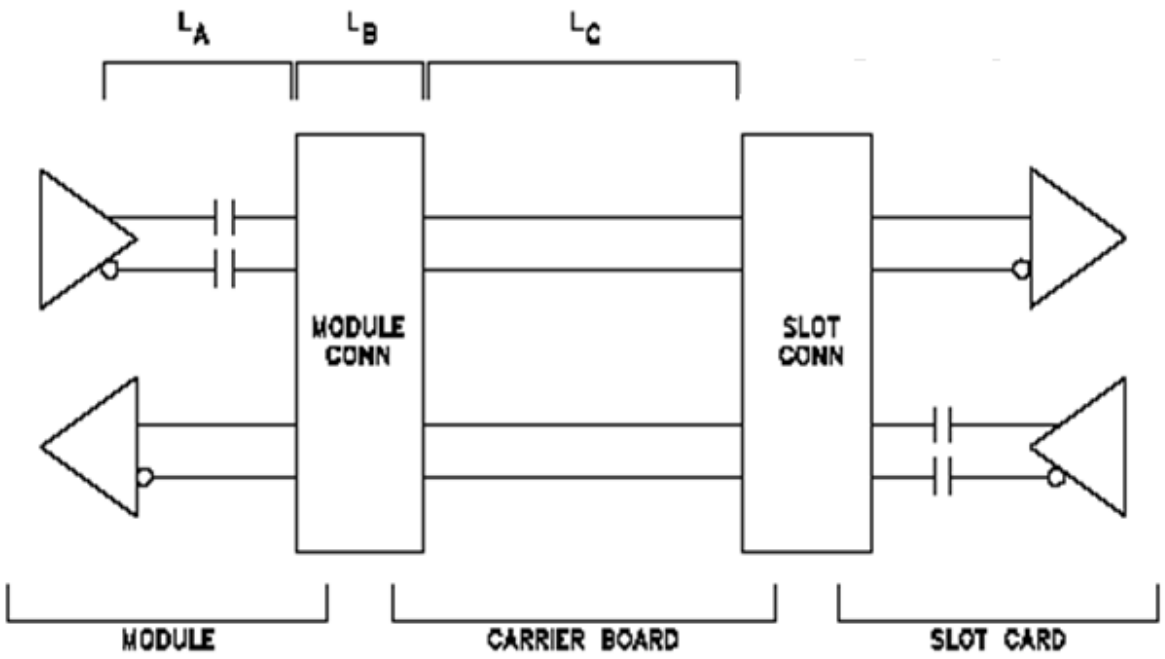


Figure 5: Topology for PCI Express Device Down.

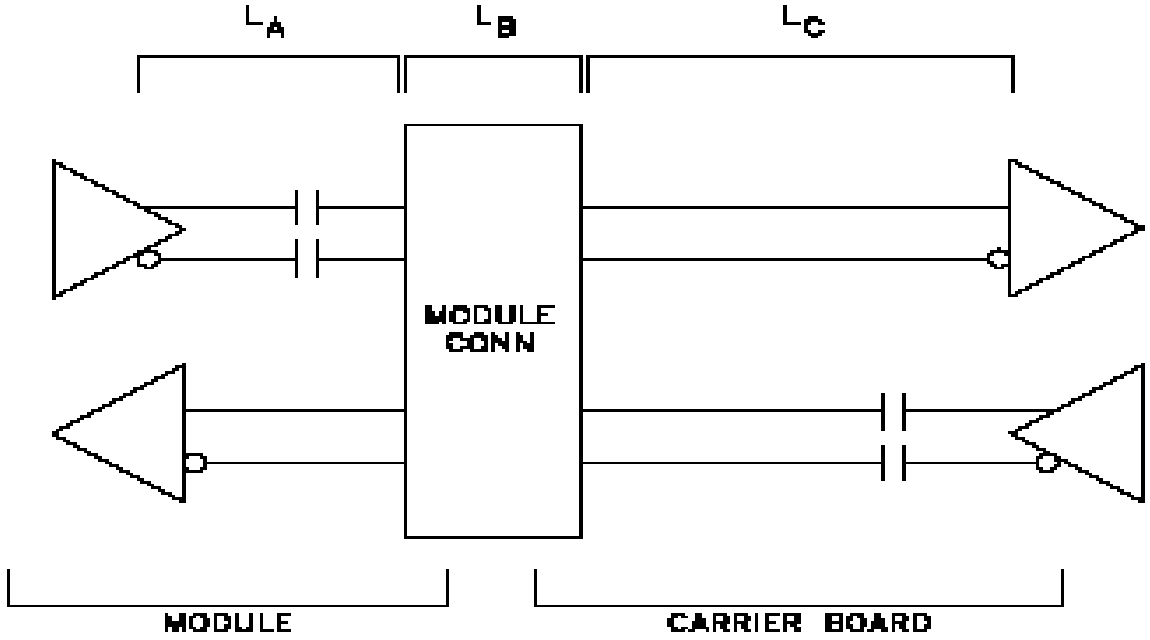


Table 8: PCI Express Gen2* Slot Card / Device Down Trace Length Guidelines

Parameter	PCI Express Gen2	Notes
Symbol Rate / PCIe Lane	5.0 G Symbols/s	
Differential Impedance Target	85Ω±10%	
Single End	50Ω±10%	
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	
Spacing from edge of plane	Min. 40mils	
LA + LB	Please see the SOM-2532 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 8.7” Device Down: 10.5”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils REFCLK+ and REFCLK- (intra-pair):Max. ±2.5mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias per TX trace, Max. 4 vias per RX trace	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the SMARC Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer SMARC Carrier Board. Capacitor type: X7R, 220nF ±10%, 16V, shape 0402.	1

Notes:

1. AC caps are recommended to be placed close to PCIe device side (avoid placing AC caps on mid-bus).

Table 9: PCI Express Gen3 * Slot Card / Device Down Trace Length Guidelines

Parameter	PCI Express Gen3	Notes
Symbol Rate / PCIe Lane	8.0 G Symbols/s	
Differential Impedance Target	85Ω±10%	
Single End	50Ω±10%	
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	
Spacing from edge of plane	Min. 40mils	
LA + LB	Please see the SOM-2532 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 7.7” Device Down: 8.7”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils REFCLK+ and REFCLK- (intra-pair):Max. ±2.5mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias / TX Max. 4 vias / RX (to device) Max. 2 vias / RX (to slot)	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the SMARC Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer SMARC Carrier Board. Capacitor type: X7R, 220nF ±10%, 16V, shape 0402.	1,

Notes:

1. AC caps are recommended to be placed close to PCIe device side (avoid placing AC cpas on mid-bus).

2.3 SERDES *SOM-2532 is Option function

SERDES is the general term for SERialized and DESerialized signals on a high-speed differential line. Many chip manufacturers use different functions on the same lines as PCIe and therefore we want to bring this surrogate use to be utilized on the module. The most common use case is here for sure (S)XGMII and therefore the implementation of one or more additional LAN ports. Other functions might also be possible. Of course, these different implementations lead to possible incompatibilities between different modules and a system designer needs to ensure, that this different functionality needs to be available on the regarding module as these are optional features.

2.3.1 SERDES Signal Definitions

Table 10: SERDES Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
PCIE_C_RX+ / SERDES_1_RX+ PCIE_C_RX- / SERDES_1_RX-	S78 S79	Differential SERDES 1 Transmit Data Pair Carrier Board: Device - Connect AC Coupling cap near SMARC to device TX. N/C if not used.	I PCIE Runtime	1
PCIE_C_TX+ / SERDES_1_TX+ PCIE_C_TX- / SERDES_1_TX-	S81 S82	Differential SERDES 1 Transmit Data Pair Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to device RX. N/C if not used	O PCIE Runtime	1
PCIE_D_RX+ / SERDES_0_RX+ PCIE_D_RX- / SERDES_0_RX-	S32 S33	Differential SERDES 0 Transmit Data Pair Carrier Board: Device - Connect AC Coupling cap near SMARC to device TX. N/C if not used.	I PCIE Runtime	1
PCIE_D_TX+ / SERDES_0_TX+ PCIE_D_TX- / SERDES_0_TX-	S29 S30	Differential SERDES 0 Transmit Data Pair Module has integrated AC Coupling Capacitor. Carrier Board: Device - Connect to device RX. N/C if not used	O PCIE Runtime	1
MDIO_CLK	S45	MDIO Signals to Configure Possible PHYs Signal for communication to a PHY	O CMOS Runtime 1.8V	1
MDIO_DAT	S46	MDIO Signals to Configure Possible PHYs Signal for communication to a PHY	I/O OD CMOS Runtime 1.8V	1

1. SEDRES is option function.

2.3.2 SERDES General Routing Guidelines

2.3.3 SERDES Trace Length Guidelines

Figure 6: Topology for SERDES Device Down.

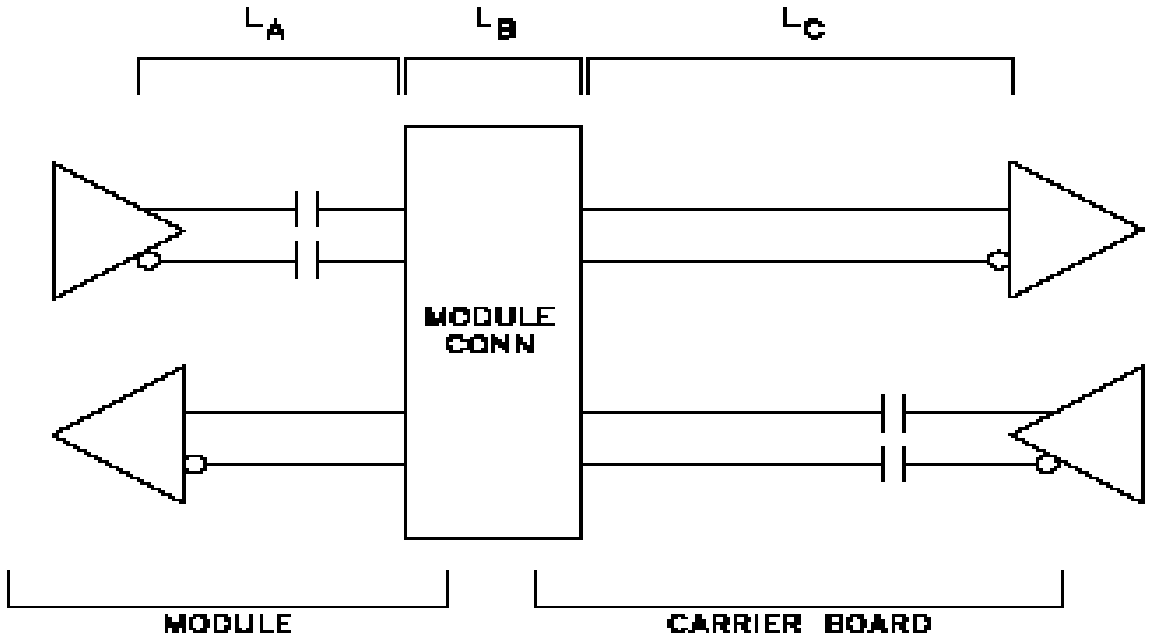


Table 11: SERDES Trace Length Guidelines

Parameter	SERDES	Notes
Symbol Rate / PCIe Lane		
Differential Impedance Target	100Ω±10%	
Single End	50Ω±10%	
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20mils	
Spacing from edge of plane	Min. 40mils	
LA + LB	Please see the SOM-2532 Layout Checklist	
Lc	Carrier Board Length	
Max length of LA+LB+LC	Slot Card: 8.1” Device Down: 10”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	
Reference Plane	GND referencing preferred Min 40-mil trace edge-to-major plane edge spacing GND stitching vias required next to signal vias if transitioning layers between GND layers Power referencing acceptable if stitching caps are used	
Carrier Board Via Usage	Max. 2 vias	
AC coupling	The AC coupling capacitors for the TX lines are incorporated on the SMARC Module. The AC coupling capacitors for RX signal lines have to be implemented on the customer SMARC Carrier Board. Capacitor type: X7R, 100nF ±10%, 16V, shape 0402.	1

Notes:

1. AC caps are recommended to be placed close to device side (avoid placing AC caps on mid-bus).

2.4 LAN Interface

The SMARC 2.11 pin-out supports two gigabit Ethernet capable ports. If only one is implemented, it should be GBE0.

Additional Ethernet capabilities may be added by utilizing the optional SERDES (See section 2.3 ‘SERDES’).

2.4.1 LAN Signal Definitions

The LAN interface of the SMARC module consists of 8 pairs of low voltage differential pair signals designated from *'GBE[0:1]_MDI0'* (+ and -) to *'GBE[0:1]_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetics to the carrier board.

Table 12: LAN Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
GBE0_MDI0+ GBE0_MDI0-	P30 P29	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used.	I/O GBE MDI Standby	
GBE0_MDI1+ GBE0_MDI1-	P27 P26	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used	I/O GBE MDI Standby	
GBE0_MDI2+ GBE0_MDI2-	P24 P23	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI2+/- N/C if not used.	I/O GBE MDI Standby	

Signal	Pin#	Description	I/O	Note
GBE0_MDI3+ GBE0_MDI3-	P20 P19	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI3+/- N/C if not used	I/O GBE MDI Standby	
GBE0_CTREF	P28	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less. Carrier Board: 0.1uF to ground. N/C if not used.	Analog Standby 0 to 3.3V max	1
GBE0_LINK_ACT#	P25	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Shall be able to sink 24mA or more Carrier LED current	O OD CMOS Standby 3.3V	
GBE0_LINK100#	P21	Link Speed Indication LED for 100Mbps ***Shall*** be able to sink 24mA or more Carrier LED current	O OD CMOS Standby 3.3V	
GBE0_LINK1000#	P22	Link Speed Indication LED for 1000Mbps ***Shall*** be able to sink 24mA or more Carrier LED current .	O OD CMOS Standby 3.3V	
GBE0_SDP	P6	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.4.2 for details.	I/O CMOS Standby 3.3V	1

Signal	Pin#	Description	I/O	Note
GBE1_MDI0+ GBE1_MDI0-	S17 S18	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used.	I/O GBE MDI Standby	
GBE1_MDI1+ GBE1_MDI1-	S20 S21	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI0+/- N/C if not used	I/O GBE MDI Standby	
GBE1_MDI2+ GBE1_MDI2-	S23 S24	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI2+/- N/C if not used.	I/O GBE MDI Standby	
GBE1_MDI3+ GBE1_MDI3-	S26 S27	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. Module has integrated termination. Carrier Board: Connect to Magnetics Module MDI3+/- N/C if not used	I/O GBE MDI Standby	
GBE1_CTREF	S28	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less. Carrier Board: 0.1uF to ground. N/C if not used.	Analog Standby 0 to 3.3V max	1

Signal	Pin#	Description	I/O	Note
GBE1_LINK_ACT#	S31	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Shall be able to sink 24mA or more Carrier LED current	O OD CMOS Standby 3.3V	
GBE1_LINK100#	S19	Link Speed Indication LED for 100Mbps ***Shall*** be able to sink 24mA or more Carrier LED current	O OD CMOS Standby 3.3V	
GBE1_LINK1000#	S22	Link Speed Indication LED for 1000Mbps ***Shall*** be able to sink 24mA or more Carrier LED current .	O OD CMOS Standby 3.3V	
GBE1_SDP	P5	Gigabit Ethernet Controller 1 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.4.2 for details.	I/O CMOS Standby 3.3V	1

Note:

1. SOM-2532 is NC.

Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes.

Some pairs are unused in some modes, per the following:

Table 13: The MDI can operate in 1000, 100 and 10 Mbit / sec modes

	1000BASE-T	100BASE-TX	10BASE-T
MDI[0]+/-	B1_DA+/-	TX+/-	TX+/-
MDI[1]+/-	B1_DB+/-	RX+/-	RX+/-
MDI[2]+/-	B1_DC/-		
MDI[3]+/-	B1_DD+/-		

2.4.2 SDP Pins

The Software Defined Pins (SDP) can be used to provide a timing communication path between the Module and Carrier. A board level signal that communicates time is a key element that facilitates clock synchronization between elements of a platform. Examples of such elements include, but are not limited to, CPU, Chipset, FPGA and others.

Modules ***should*** connect the SDP signal to a module element pin capable of propagating (transmitting) time, and/or time-stamping (receiving) the signal to extract time information from it. If implemented, the direction of the signal with respect to the module element ***should*** be able to be determined by system software.

Pulse Per Second (PPS):

A PPS signal conveys both frequency and phase and can be used to transfer time information between elements within a platform. It is commonly used because it encapsulates both frequency and time into a single signal. It is preferred over other methods that require more complex implementations of hardware and software. A GPS is probably the most widespread, high-quality, clock source capable of generating a PPS signal.

Platform-level Synchronization Implementation Examples:

Example1: The Network Interface Controller (NIC) on the SMACR Module is Precision Time Protocol (PTP) capable and the SMARC designer has connected a software configurable, timing aware, pin on the NIC to the SDP pin on the module/carrier interface. Software can configure the NIC to output a PPS signal onto this pin that connects it to one or more elements on the module and/or carrier board.

Example2: The carrier board has provisions for connecting a PPS output from a GPS to the SDP signal connection to the module. The module element (i.e. NIC, CPU, Chipset) can receive the timing information from the carrier board and adjust its time accordingly.

Precision Time Protocol - Background

Standards such as IEEE 1588, 802.1AS, and Time Sensitive Networking (TSN) provide standards for synchronizing time between nodes on a local area network. Additional benefits of the standards may include lower latency and improved network traffic Quality of Service (QoS). Systems that commonly require synchronization include those made up of distributed nodes that perform measurement, control, and compute functions. These nodes may have clock sources with varying degrees of accuracy and stability.

System-wide time synchronization with sub-microsecond accuracy is supported, by PTP standards, with minimal network and compute resource utilization.

It is the merger of the platform-level synchronization and network level synchronization pieces that enable real-time distributed systems. Additional information regarding the aforementioned standards can be found in their respective specifications and widely available supporting documents.

Software Implementation:

The software architecture and features required to support platform and network level synchronization are outside the scope of this specification.

2.4.3 LAN Implementation Guidelines

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the SMARC module. It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a SMARC module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

2.4.4 LAN Magnetics Modules

1000Base-T Ethernet magnetics modules are similar to those designed solely for 10/100 BaseTx Ethernet, except that there are four MDI differential signal pairs instead of two. 1000Base-T magnetics modules have a center tap pin that is connected to the reference voltage output *'GBE_CTREF'* of the SMARC module, which biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with one or two center tap pins. Depending on the PHY manufacturer some PHYs may require, that each differential pair center tap pin is connected separately via a capacitor to ground. In this case the PHY center tap pins are not connected together.The isolation magnetics can be integrated in a RJ45 jack, which also provides activity and speed LED indicators. Alternatively, they can be designed as discrete magnetics modules, which will be connected to a pure RJ45 jack.

2.4.5 LAN Component Placement

When using RJ45 connectors without integrated magnetics, the discrete magnetics module has to be placed as close as possible to the RJ45 connector. The distance between the magnetics module and RJ45 connector must be less than 1 inch. This distance requirement must be observed during the carrier board layout when implementing LAN. Due to the insertion loss budget of SMARC, the overall trace length of the MDI signal pairs on the carrier board should be less than 4 inches. Signal attenuation could cause data transfer problems for traces longer than 4 inches.

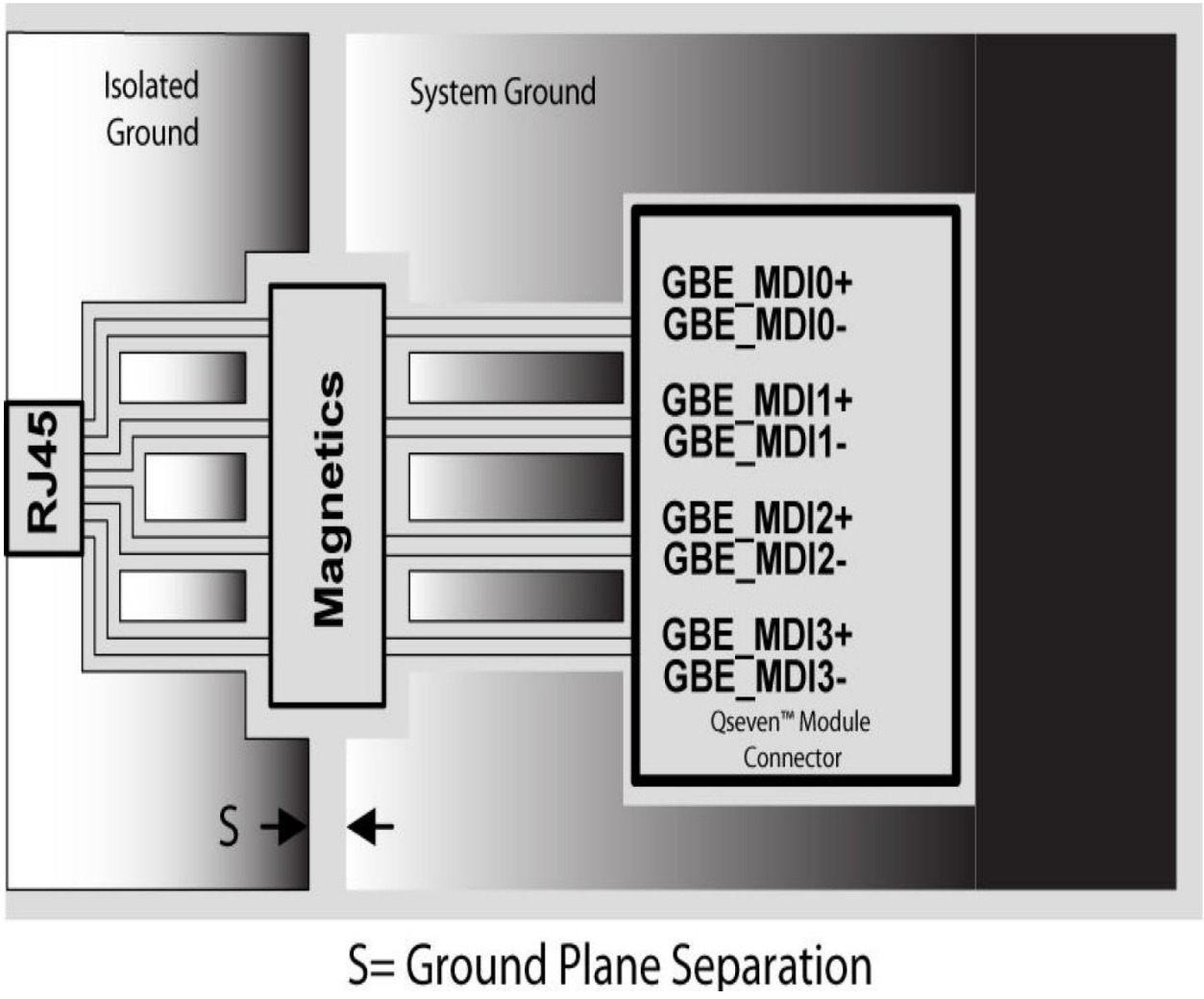
2.4.6 LAN Ground Plane Separation

Isolated separation between the analog ground plane and digital ground plane is recommended. If this is not implemented properly then bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to ground bounce noise.

The plane area underneath the magnetic module should be left empty. This free area is to keep transformer induced noise away from the power and system ground planes.

The isolated ground, also called chassis ground, connects directly to the fully shielded RJ45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection, a 3kV high voltage capability capacitor is recommended to connect to this chassis ground.

Figure 7: LAN Ground Plane Separation



2.4.7 LAN Link Activity and Speed LED

The SMARC module has four 3.3V push/pull outputs to directly drive activity, speed indication and link status LEDs. The 3.3V standby voltage should be used as LED supply voltage so that the link activity can be viewed during system standby state. Since LEDs are likely to be integrated into a RJ45 connector with integrated magnetics module, the LED traces need to be routed away from potential sources of EMI noise. Consider adding a filtering capacitor per LED for extremely noisy situations. The suggested value for this capacitor is 470pF.

Figure 8: GBE LED Current Sink

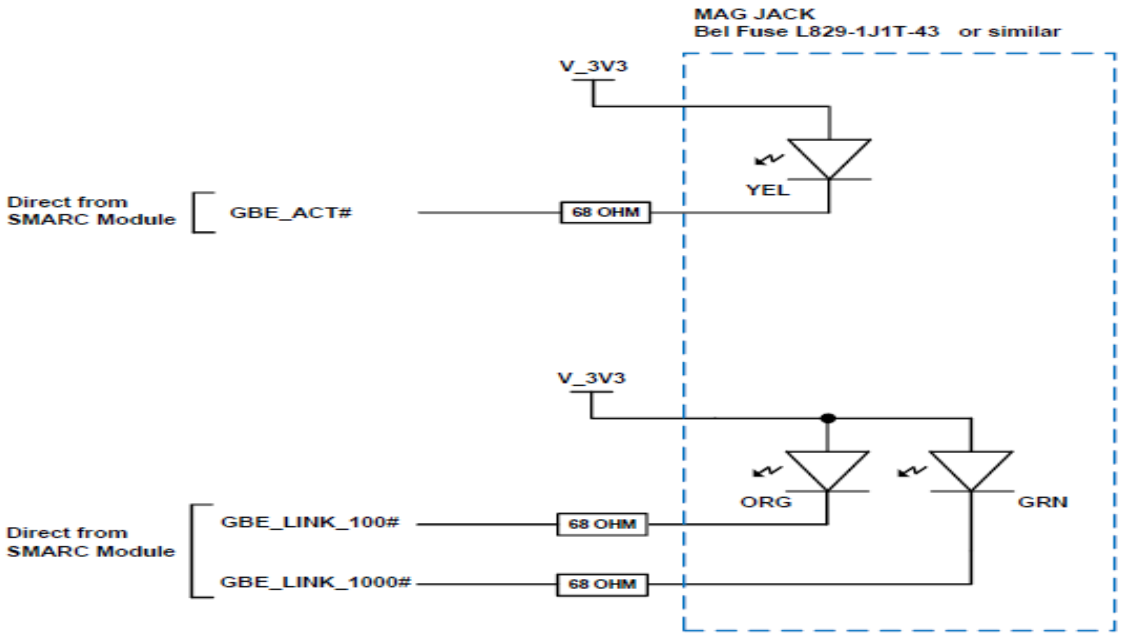
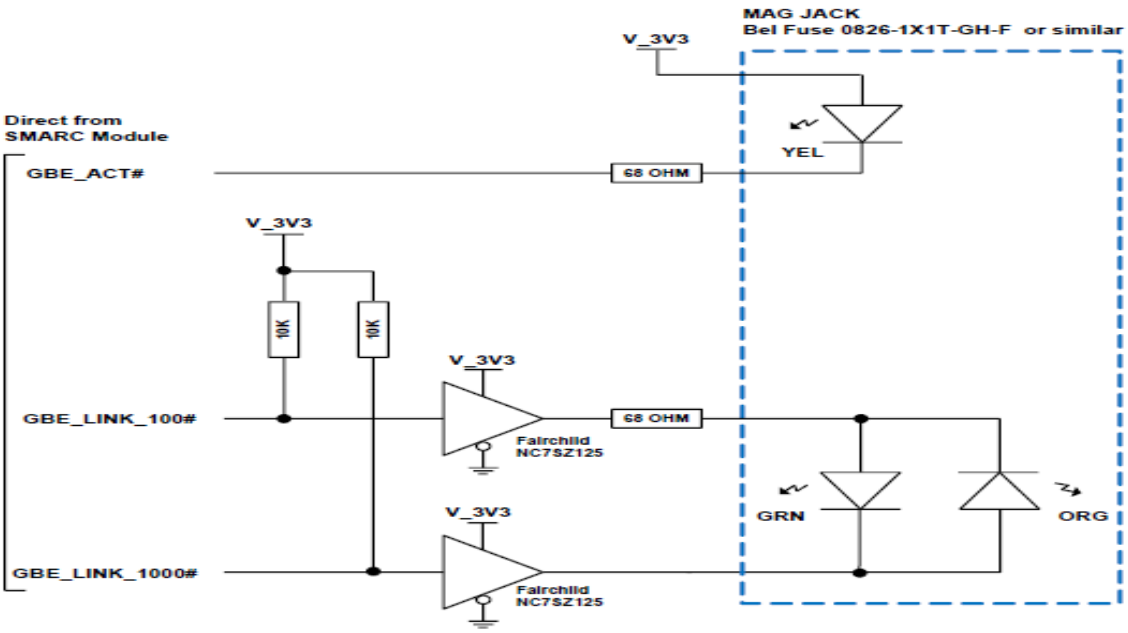


Figure 9: GBE LED Current Sink / Source



2.4.8 LAN Trace Length Guidelines

Figure 10: Topology for Ethernet Jack

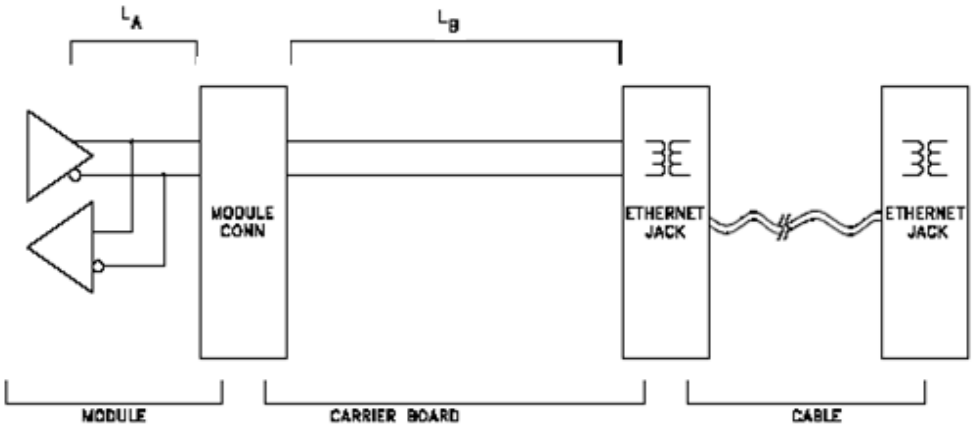


Table 14: Ethernet Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	GBE0_MDIx+, GBE0_MDIx-	
Differential Impedance Target	100 Ω ±10%	
Single End	50Ω ±10%	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50mils	
Spacing between differential pairs and high-speed periodic signals	Min. 100mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 50mils	
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 100mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	SMARC Module to the magnetics Module - 5.0 inches. Magnetics Module to RJ45 connector - Max. 1.0 inches.	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils MDI+ and MDI- pairs (inter-pair) - Max. ±500mils	
Reference Plane	GND referencing preferred..	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias.	

Notes:

2.4.9 Reference Ground Isolation and Coupling

The Carrier Board should maintain a well-designed analog ground plane around the components on the primary side of the transformer between the transformer and the RJ-45 receptacle. The analog ground plane is bonded to the shield of the external cable through the RJ-45 connector housing.

The analog ground plane should be coupled to the carrier's digital logic ground plane using a capacitive coupling circuit that meets the ground plane isolation requirements defined in the 802.3-2005 specification. It is recommended that the Carrier Board PCB design maintain a minimum 30 mil gap between the digital logic ground plane and the analog ground plane.

It's recommended to place an optional GND to SHIELDGND connection near the RJ-45 connector to improve EMI and ESD capabilities.

2.5 SATA

The Module definition allows for one SATA port. The port *may* be SATA Gen 1, 2 or 3 as the Module chip or chipset allows.

The Carrier SATA device *may* be selected as the Boot Device – see *Section 2.22*

2.5.1 SATA Signal Definitions

Table 15: SATA Signal Definitions

Signal	Pin#	Description	I/O	Note
SATA_RX+ SATA_RX-	P51 P52	Serial ATA , Receive input differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 6 RX+ Connect to SATA0 Conn pin 5 RX- N/C if not used.	I SATA Runtime	
SATA_TX+ SATA_TX-	P48 P49	Serial ATA , Transmit output differential pair. Module has integrated AC Coupling capacitor Carrier Board: Connect to SATA0 Conn pin 2 TX+ Connect to SATA0 Conn pin 3 TX- N/C if not used.	O SATA Runtime	
SATA_ACT#	S54	Serial ATA activity LED. Open collector output pin driven during SATA command activity. Module has integrated PU resistor Carrier Board: Connect to LED and current limiting resistors 250 to 330 Ω to 3.3V N/C if not used.	O OD CMOS Runtime 3.3V	Able to drive 24 mA

Notes:

2.5.2 SATA Application

If customer want to design mSATA/MO-300 and M.2 (B keying, M keying and E keying), please refer Section 5.4 SATA of SMARC Design Guide 2.0 from page 81 to page 86.

2.5.3 SATA Routing Guidelines

2.5.3.1 General SATA Routing Guidelines

Use the following general routing and placement guidelines when laying out a new design.

- SATA signals must be ground referenced. If changing reference plane is completely unavoidable (that is, ground reference to power reference), proper placement of stitching caps can minimize the adverse effects of EMI and signal quality performance caused by reference plane change. Stitching capacitors are small valued capacitors (1 µF or lower in value) that bridge the power and ground planes close to where a high-speed signal changes layers. Stitching caps provide a high frequency current return path between different reference planes. They minimize the impedance discontinuity and current loop area that crossing different reference planes created. The maximum number allowed for SATA to change reference plane is one.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided.
- Minimize layer changes. If a layer change is necessary, ensure that trace matching for either transmit or receive pair occurs within the same layer. Intel recommends to use SATA vias as seldom as possible.
- **DO NOT** route SATA traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- **DO NOT** place stubs, test points, test vias on the route to minimize reflection. Utilize vias and connector pads as test points instead.
- For testability, route the TX and RX pairs for a given port on the same layer and close to each other to help ensure that the pairs share similar signaling characteristics. If the groups of traces are similar, a measure of RX pair layout quality can be approximated by using the results from actively testing the TX pair's signal quality.
- Length matching rules are required on SATA differential signals for optimum timing margins, preventing common-mode signals and EMI. Each net within a differential pair should be length matched on a segment-by-segment basis at the point of discontinuity. Total length mismatch must not be more than 20 mils (0.508 mm). Examples of segments might include breakout areas, routes running between two vias, routes between an AC coupling capacitor and a connector pin, etc. The points of discontinuity would be the via, the capacitor pad, or the connector pin. Matching of TX and RX within the same port and between SATA TX and RX pairs from differential ports is not required. When length matching compensation occurs, it should be made as close as possible to the point where the variation occurs.
- **DO NOT** serpentine to match RX and TX traces; there is **NO** requirement to match RX and TX traces. In addition, **DO NOT** serpentine to meet minimum length guidelines on RX and TX traces.
- Recommend keeping SATA traces 20 mils (0.508 mm) from any vias on the motherboard whenever possible.

2.5.3.2 SATA Differential Transitional Via Recommendations

Please refer to 2.2.4.1

2.5.4 SATA Trace Length Guidelines

Figure 11: Topology for SATA

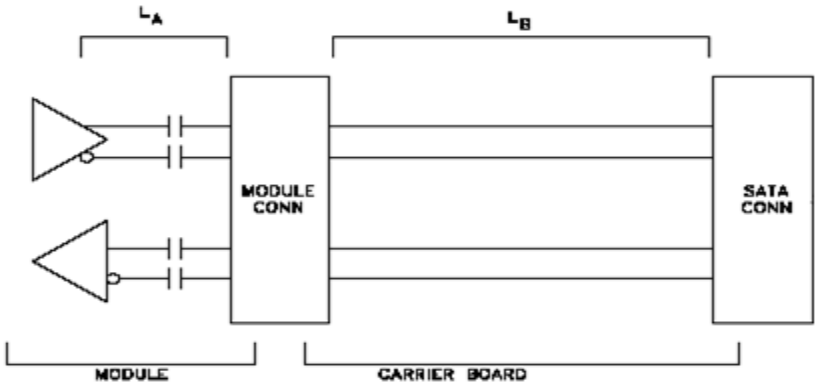


Table 16: SATA Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SATA	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Signal length available for the SMARC Carrier Board	3 inches, a redriver may be necessary for GEN3 signaling rates	
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	5.7”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	A maximum of 2 vias is recommended.	
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are implemented on the SMARC module.	

Notes:

2.6 USB Interface

General:

The USB (Universal Serial Bus) is a hot-pluggable general purpose high speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin. Additionally a fifth pin, USB ID (mostly used in devices supporting USB-OTG), may also be used which indicates whether the device operates in Host mode or a Client/Device mode.

SMARC 2.0 provides six sets of USB 2.0 signals and two sets of USB 3.2 Super Speed signals. USB OTG and USB Client functionalities are also supported.
USB 3.2 is supported for the USB ports 2 and 3. For implementation of USB 3.2 OTG or USB 3.2 host USB3 may be used.
The order follows the port prefixes USB0 to USB5. For USB 3.2 SuperSpeed signals the filling order is USB2 to USB3.
At least one USB client port should be supported. It may also be available as an OTG port. There can be one or two USB client ports. If one USB client port is supported it can be port 0 or port 3.
USB 3.2 Gen. 1 with 5 Gbit/s is supported. Support for USB 3.2 Gen 2 with 10 Gbit/s might be supported in the future. Limitation for trace length will apply. USB 3.2 Gen. 2 x 2 is not supporteded.

2.6.1 USB Signal Assignments

Table 17: USB Signal Assignments

	USB 2.0	USB 3.2	OTG/VBUS	Client Capability
USB0	may[1]		may	should
USB1	shall			
USB2	may	may		
USB3	may	may	may	may
USB4	may			
USB5	may			

1. USB0 ***shall*** be implemented as Host or OTG/Client

2.6.2 USB2.0 Signal Definitions

Table 18: USB2.0 Signal Descriptions

Signal	Pin#	Description	I/O	Note
USB0+ USB0-	P60 P61	USB Port 0, data + or D+ USB Port 0, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	
USB1+ USB1-	P65 P66	USB Port 1, data + or D+ USB Port 1, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	
USB2+ USB2-	P69 P70	USB Port 2, data + or D+ USB Port 2, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	
USB3+ USB3-	S68 S69	USB Port 3, data + or D+ USB Port 3, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	
USB4+ USB4-	S35 S36	USB Port 4, data + or D+ USB Port 4, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	

Signal	Pin#	Description	I/O	Note
USB5+ USB5-	S59 S60	USB Port 5, data + or D+ USB Port 5, data + or D- Carrier board: Device - Connect to D+/- Conn. - Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to Pin 3 D+ / Pin 2 D- N/C if not used	I/O USB Standby USB	

Signal	Pin#	Description	I/O	Note
USB0_EN_OC#	P62	USB over-current sense, USB ports 0 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.5.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1
USB1_EN_OC#	P67	USB over-current sense, USB ports 1 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.6.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1

Signal	Pin#	Description	I/O	Note
USB2_EN_OC#	P71	USB over-current sense, USB ports 2 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.6.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1
USB3_EN_OC#	P74	USB over-current sense, USB ports 3 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.6.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1
USB4_EN_OC#	P76	USB over-current sense, USB ports 4 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.6.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1

Signal	Pin#	Description	I/O	Note
USB5_EN_OC#	S55	USB over-current sense, USB ports 5 Pulled low by Carrier OD driver to indicate over-current situation. This signal has 10K Ω pull up to 3.3V_DUAL on the module. The pull-up rail may be switched off to conserve power if the USB port is not in use. Further details may be found in Section 2.6.2.1 USB[0:5]_EN_OC# Discussion below. Carrier Board: Connect to Overcurrent of Power Distribution Switch and Bypass 0.1uF to GND N/C if not used	I/O OD COMS Standby 3.3V	1
USB0_OTG_ID	P64	USB OTG ID pin. Configures the mode of the USB Port 0. The resistance of this pin measured to ground is used to determine whether USB Port 0 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details. Carrier Board: Client - PU 100KΩ to 3.3VSB Host - PD 100KΩ to GND	Standby	
USB3_OTG_ID	S104	USB OTG ID pin. Configures the mode of the USB Port 3. The resistance of this pin measured to ground is used to determine whether USB Port 3 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details. Carrier Board: Client - PU 100KΩ to 3.3VSB Host - PD 100KΩ to GND	I COMS Standby 3.3V	2

Signal	Pin#	Description	I/O	Note
USB0_VBUS_DET	P63	USB host power detection, when this port is used as a device.	I USB VBUS Standby 5V	
USB3_VBUS_DET	S37	USB host power detection, when this port is used as a device.	I USB VBUS Standby 5V	2

Notes:

1. 3.3V or switched 3.3V: if a USB channel is not used, then the USB[0:5]_EN_OC# pull-up rail may be held at GND to prevent leakage currents.

2. SOM-2532 is NC pin.

2.6.2.1 USB[0:5]_EN_OC# Discussion

The Module USB[0:5]_EN_OC# pins are multi-function Module pins, with a pull-up to a 3.3V rail on the Module, an OD driver on the Module, and, if the OC# (over-current) monitoring function is implemented on the Carrier, an OD driver on the Carrier. The use is as follows:

1) On the Carrier board, for external plug-in USB peripherals (USB memory sticks, cameras, keyboards, mice, etc.) USB power distribution is typically handled by USB power switches such as the Texas Instruments TPS2052B or the Micrel MIC2026-1 or similar devices. The Carrier implementation is more straightforward if the Carrier USB power switches have active–high power enables and active low open drain OC# outputs (as the TI and Micrel devices referenced do). The USB power switch Enable and OC# pins for a given USB channel are tied together on the Carrier. The USB power switch enable pin must function with a low input current. The TI and Micrel devices referenced above require 1 microampere or less, at a 3.3V enable voltage level.
2) The Module drives USB[0:5]_EN_OC# low to disable the power delivery to the USB[0:5] device.
3) The Module floats USB[0:5]_EN_OC# to enable power delivery. The line is pulled to 3.3V by the Module pull-up, enabling the Carrier board USB power switch. If there is a USB over-current condition, the Carrier board USB power switch drives the USB[0:5]_EN_OC# line low. This removes the over-current condition (by disabling the USB switch enable input), and allows Module software to detect the over-current condition. The Module software ***should*** look for a falling edge interrupt on USB[0:5]_EN_OC#, while the port is enabled, to detect the OC# condition. The OC# condition will not last long, as the USB power switch is disabled when the switch IC detects the OC# condition. If the USB power to the port is disabled (USB[0:5]_EN_OC# is driven low by the Module) then the Module software must be aware that the port is disabled, and the low input value on the port does not indicate an over-current condition (because the port power is disabled).If the USB power to the port is disabled, then the Module ***may*** remove the 3.3V pull-up voltage to the USB[0:5]_EN_OC# node, to save the current drain through the pull-up resistor. This is optional and Module design dependent.

Carrier Board USB peripherals that are not removable often do ***not*** make use of USB power switches with current limiting and over-current detection. It is usually deemed un-necessary for non-removable devices. In these cases, the USB[0:5]_EN_OC# pins ***may*** be left unused, or they ***may*** be used as USB[0:5] power enables, without making use of the over-current detect Module input feature.

2.6.2.2 Powering USB devices during S5

The power distribution switches and the ESD protection shown in the schematics can be powered from Main Power or Suspend Power (VCC_5V_SBY). Ports powered by Suspend Power are powered during the S3 and S5 system states.

2.6.3 USB2.0 Routing Guidelines

2.6.3.1 USB 2.0 General Design Considerations and Optimization

Use the following general routing and placement guidelines when laying out a new design. These guidelines help minimize signal quality and EMI problems.

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Separate signal traces into similar categories, and route similar signal traces together (such as routing differential-pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20 x h rule by keeping traces at least [20 x (height above the plane)] mils away from the edge of the plane (VCC or GND). For an example stackup, the height above the plane is 4.5 mils (0.114 mm). This calculates to a 90-mil (2.286-mm) spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.
- Avoid stubs on high-speed USB signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils (5.08 mm).

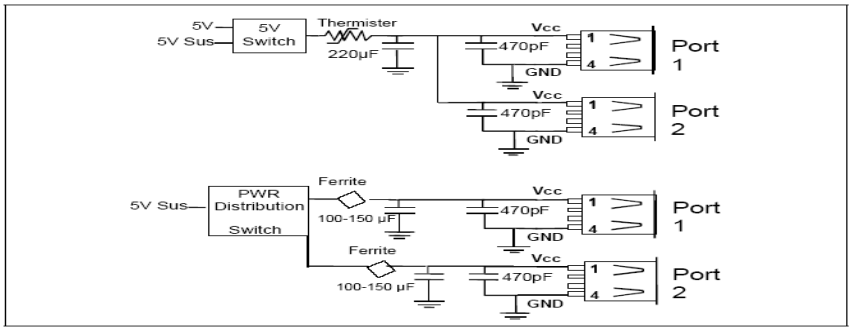
2.6.3.2 USB 2.0 Port Power Delivery

The following is a suggested topology for power distribution of VBUS to USB ports.

These circuits provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach fly back protection. These two types require both bulk capacitance (droop) and filtering capacitance (for dynamic detach fly back voltage filtering). Intel recommends the following:

- Minimize the inductance and resistance between the coupling capacitors and the USB ports.
- Place capacitors as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane.
- Make the power-carrying traces wide enough that the system fuse blows on an over current event. If the system fuse is rated at 1 A, then the power-carrying traces should be wide enough to carry at least 1.5 A.

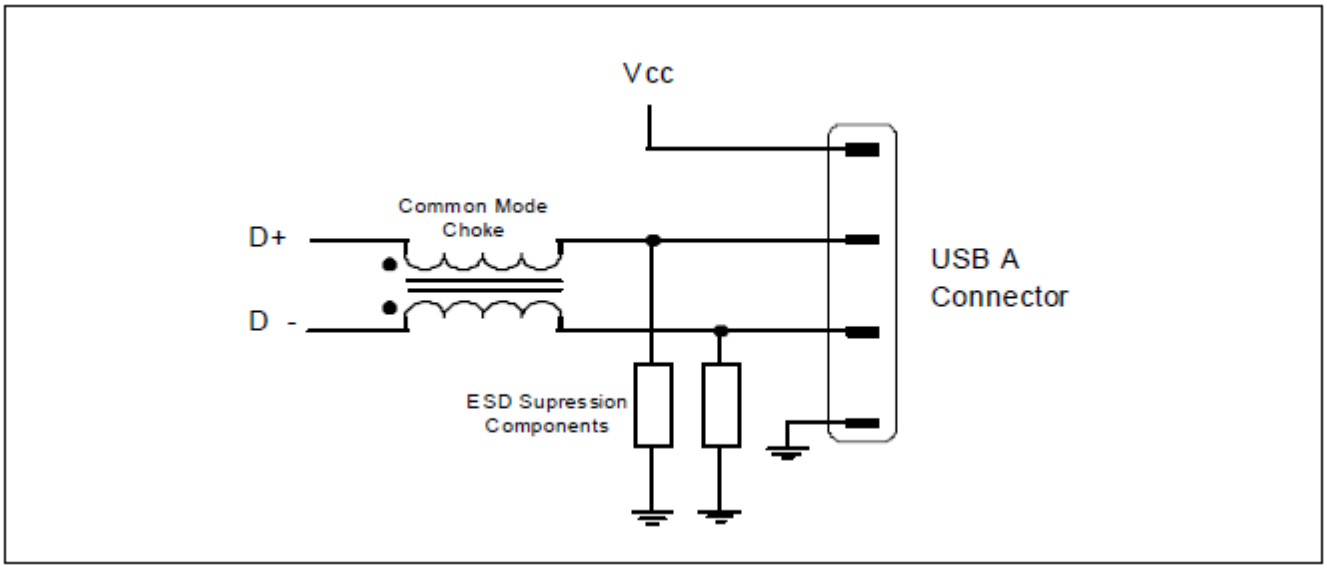
Figure 12: USB 2.0 Good Downstream Power Connection



2.6.3.3 USB 2.0 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. Place the choke as close as possible to the USB connector signal pins.

Figure 13: USB 2.0 A Common Mode Choke



Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, therefore test the effects of the common mode choke on full speed and high-speed signal quality. Common mode chokes with a target impedance of 80 Ω to 90 Ω, at 100 MHz, generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process:

1. Choose a part with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that should be suppressed.
2. After obtaining a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and highspeed USB operation.

Further common mode choke information can be found on the high-speed USB Platform Design Guides available at www.usb.org.

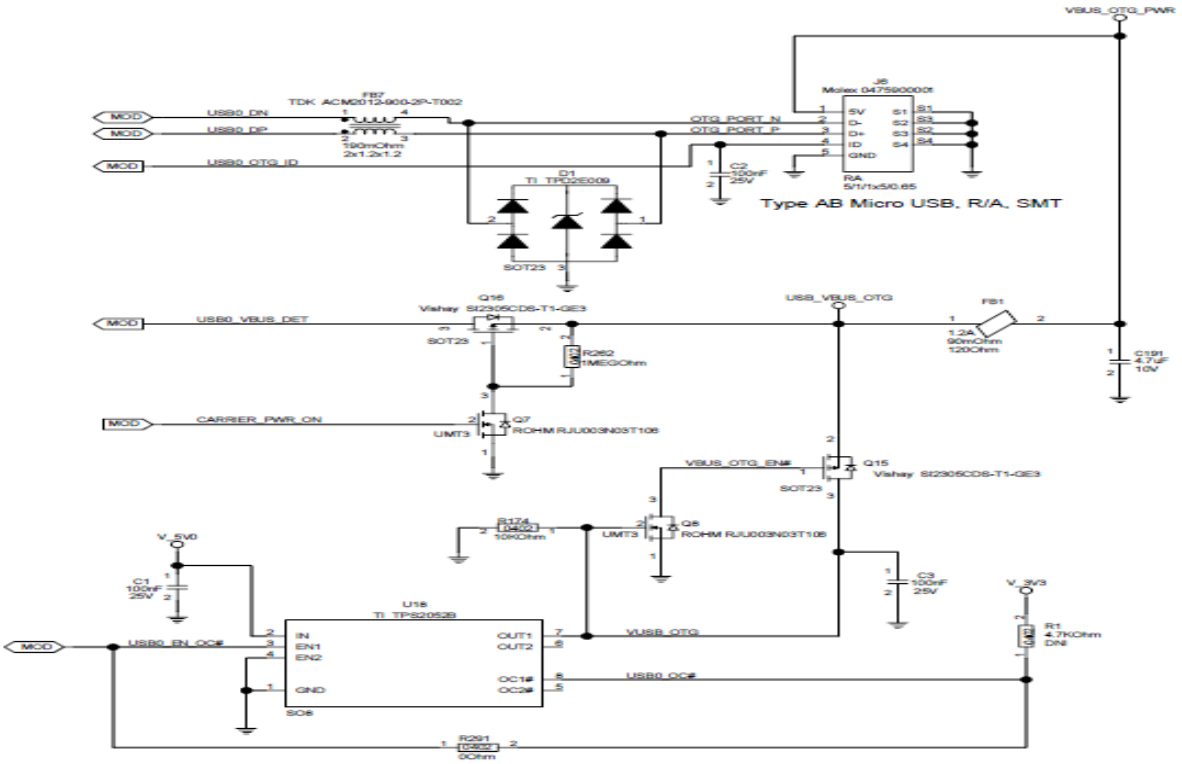
2.6.3.4 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.
Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.6.3.5 USB0 Client / Host Direct From Module

The figure below shows a USB-OTG implementation on the USB0 port terminated on a micro USB Type A/B connector
The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub. If the client device is bus powered, the Carrier can supply 5V, 500mA power to the client device. The Module USB0_EN_OC# signal controls the power switch and current limiter, the Texas Instruments TPS2052, which in turn supplies power to a bus-powered client device. Per the USB specification, bus powered USB 2.0 devices are limited to a maximum of 500 mA. The TPS2052 limits the current and can stand an indefinite short circuit to GND. The current limiting is somewhat imprecise, and kicks in between 500 mA and 1A.
Figure 14: USB0 Client / Host Direct From Module



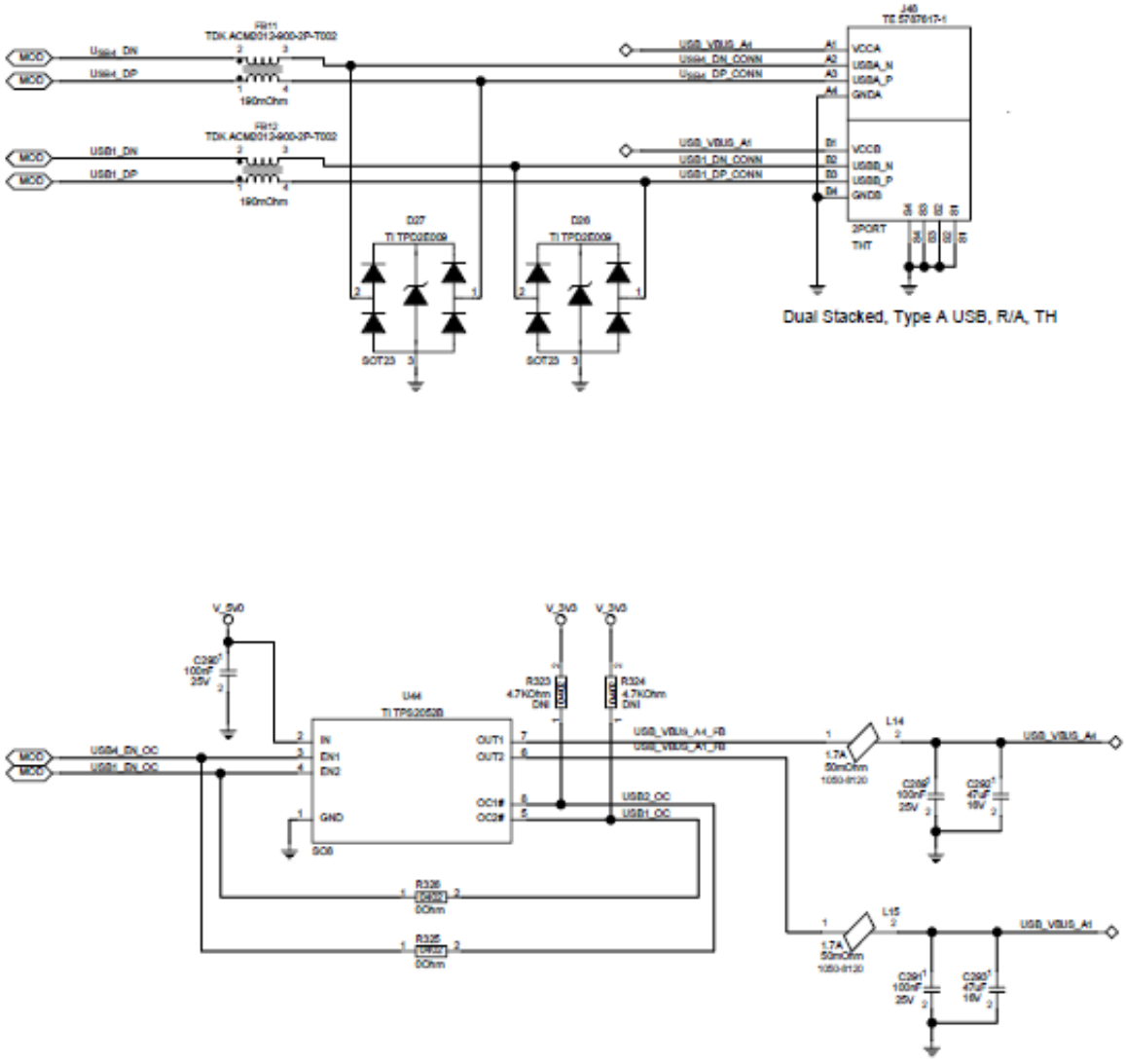
2.6.3.6 USB1 and USB2 Host Ports direct from Module

Carrier board implementation of USB host ports from SMARC USB1 and USB4 is straightforward. An implementation of a dual USB Type A Host port header is shown in the figure below.

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub.

If the target USB devices are “down” on the Carrier, then much or all of this circuit may be omitted. The SMARC USB pairs are routed directly to the target device. The ferrite choke in the USB lines, the ESD diodes, and the TPS2052 power switch and associated passives may be eliminated. However, in some cases, it is desirable to have the capability to “power cycle” a USB peripheral under software control. If this is the case, it might be desirable to retain the TPS2052 power switch, or a similar device for 3.3V power switching, with the power control function performed by the USB1_EN_OC or USB4_EN_OC, as appropriate.

Figure 15: USB1 and USB4 Host Ports Direct From Module



2.6.4 USB2.0 Trace Length Guidelines

Figure 16: Topology for USB2.0

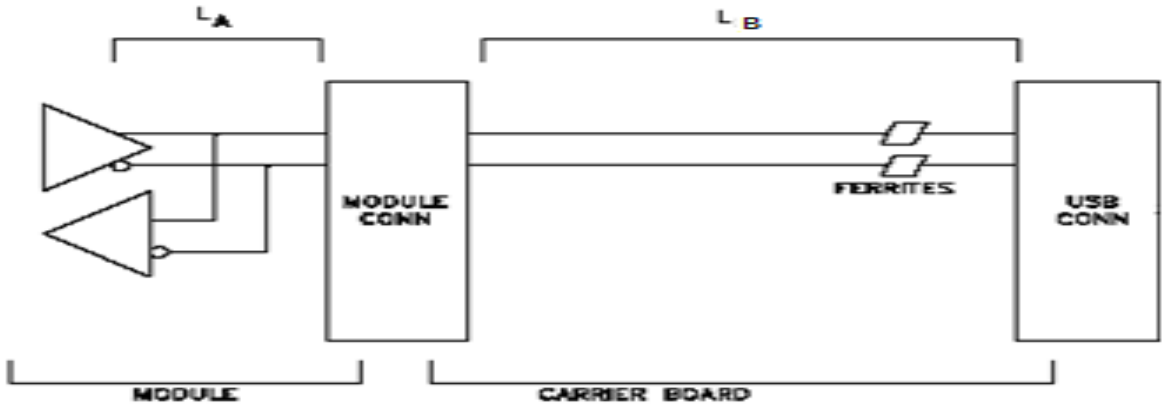


Table 19: USB2.0 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB[0:5]+, USB[0:5]-	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	12”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Try to minimize number of vias	

Notes:

2.6.5 USB3.2 *General:*

USB 3.2 is the third major revision of the Universal Serial Bus (USB) standard for computer connectivity. It adds a new transfer speed called SuperSpeed (SS) to the already existing LowSpeed (LS), FullSpeed (FS) and HighSpeed (HS).

USB 3.2 leverages the existing USB 2.0 infrastructure by adding two additional data pair lines to allow a transmission speed up to 10 Gbit/s, which is 20 times faster than USB 2.0 with 480 Mbit/s.

The additional data lines are unidirectional instead of the bidirectional USB 2.0 data lines. USB 3.2 is fully backward compatible to USB 2.0. USB 3.2 connectors are different from USB 2.0 connectors. The USB 3.2 connector is a super set of a USB 2.0 connector, with 4 additional pins that are invisible to USB 2.0 connectors. A USB 2.0 Type A plug may be used in a USB 3.2 Type A receptacle, but the USB 3.2 SuperSpeed functions will not be available.

2.6.6 USB3.2 Signal Definitions

Table 20: USB3.0 Signal Definitions

Signal	Pin#	Description	I/O	Note
USB2_SSRX+ USB2_SSRX-	S74 S75	USB Port 2, SuperSpeed RX + USB Port 2, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near SMARC to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I USB SS Standby	
USB2_SSTX+ USB2_SSTX-	S71 S72	USB Port 2, SuperSpeed TX + USB Port 2, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O USB SS Standby	

Signal	Pin#	Description	I/O	Note
USB3_SSRX+ USB3_SSRX-	S65 S66	USB Port 3, SuperSpeed RX + USB Port 3, SuperSpeed RX – Carrier Board: Device - Connect AC Coupling Capacitors 100nF near SMARC to StdA_SSTX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 6 StdA_SSRX+ / Pin 5 StdA_SSRX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	I USB SS Standby	
USB3_SSTX+ USB3_SSTX-	S62 S63	USB Port 3, SuperSpeed TX + USB Port 3, SuperSpeed TX – Module has integrated AC Coupling Capacitors Carrier Board: Device - Connect to StdA_SSRX+/- Conn. - Connect 0Ω and 90Ω @100MHz USB3.0 Common Mode Choke(NL) combined in series and USB3.0 ESD suppressors to GND to Pin 9 StdA_SSTX+ / Pin 8 StdA_SSTX-, the value of CMC depends on EMI and signal integrity performance. N/C if not used	O USB SS Standby	

Note:

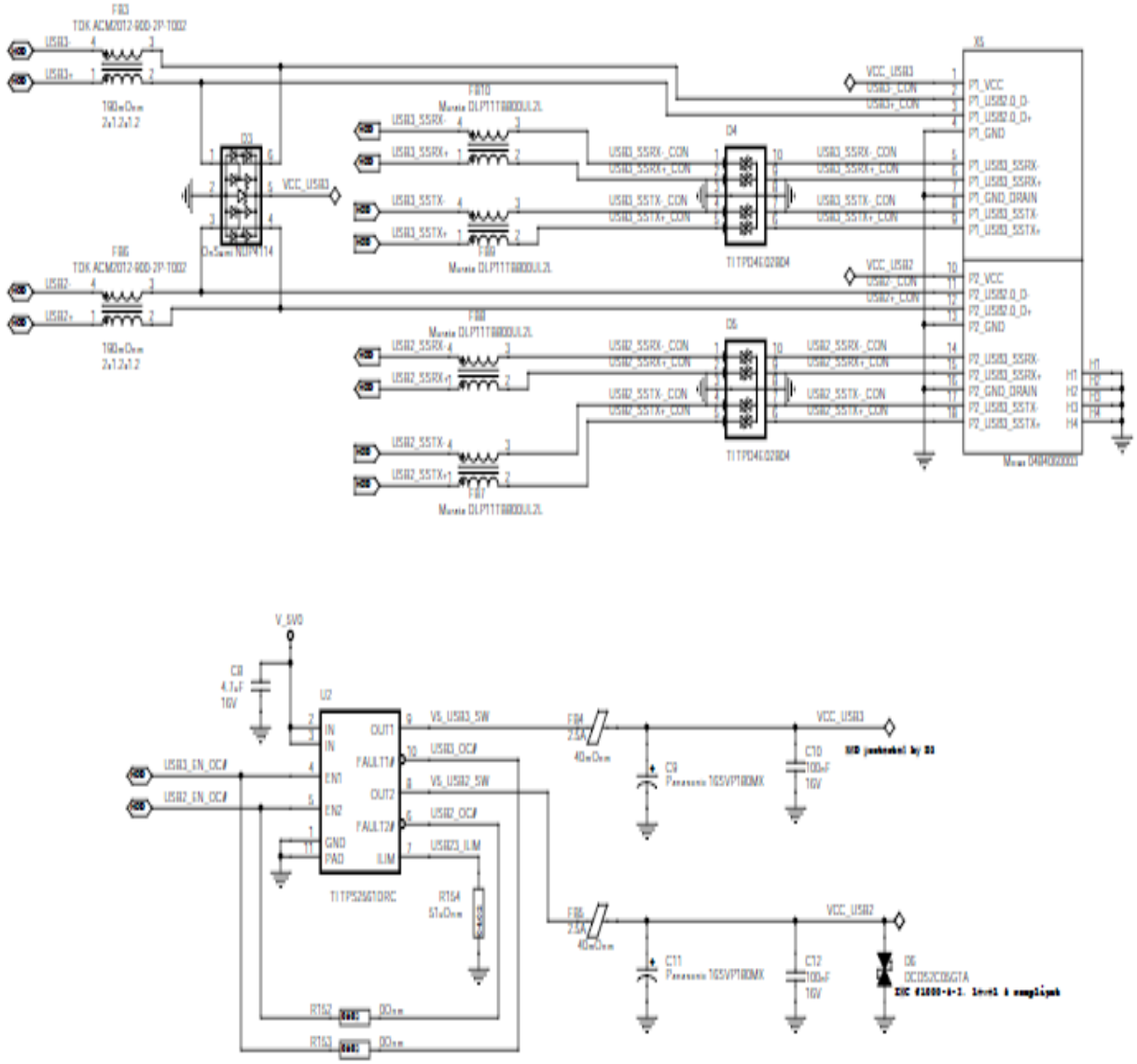
2.6.7 USB3.2 Routing Guidelines

A USB 3.2 port consists of a USB 2.0 port and a set of unidirectional SuperSpeed signals. The following example shows an implementation of a stacked dual USB 3.2 connector that is utilizing USB2 and USB3 without using the optional OTG capabilities of USB3.

Place the ESD diodes as close as possible to the connector. For SuperSpeed Signals, ESD diodes with optimized package and low I/O capacitance should be used to create only minimal impact on signal integrity. Also the common mode chokes should be selected carefully. Ensure that their differential mode cutoff frequency is well above the maximum frequency of 2.5 GHz of a USB3.0 signal.

Each USB 3.2 port should be able to supply up to 900mA and should be decoupled with at least 120µF of low ESR capacitance.

Figure 17: USB 3.2 host dual



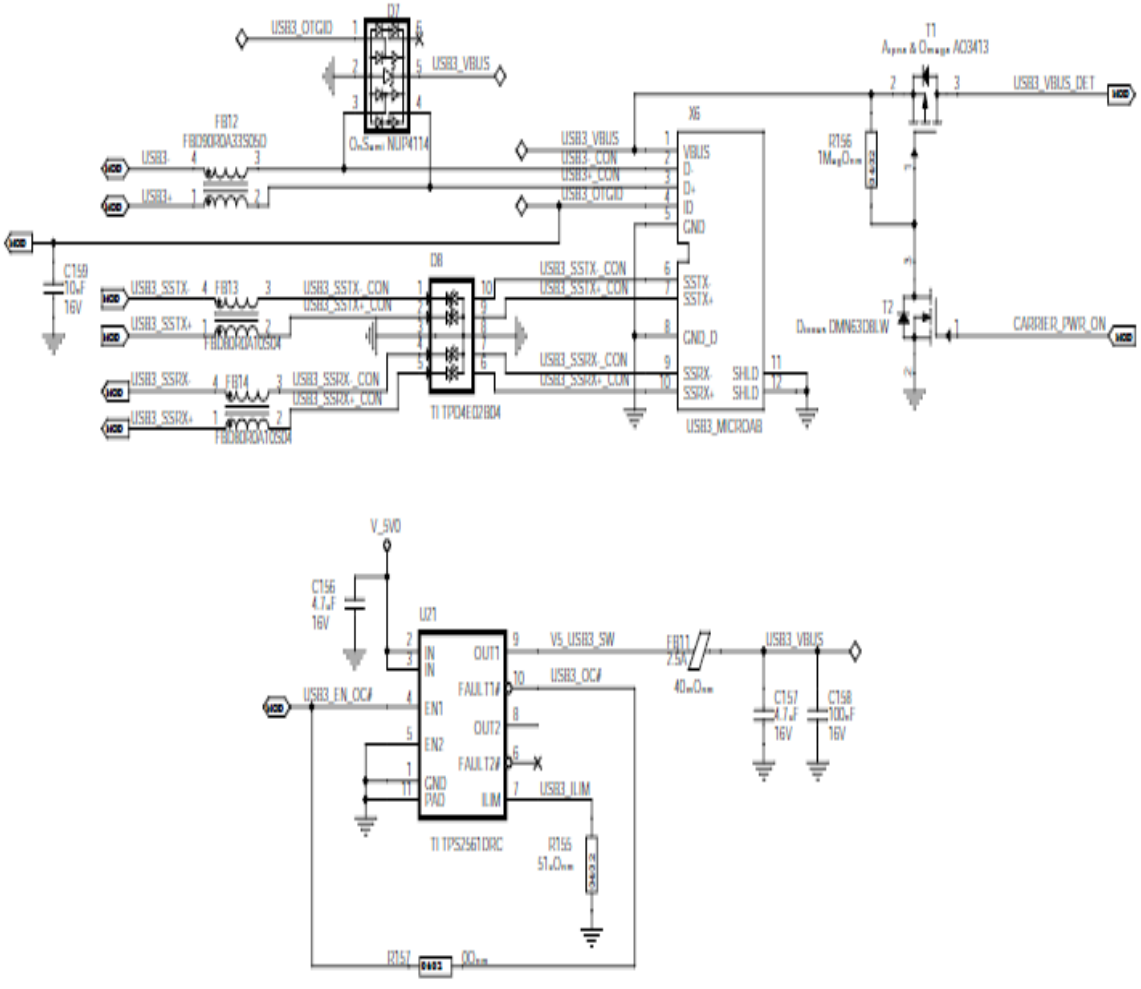
2.6.7.1 USB3.2 OTG

USB3 may support OTG functionality, depending on Module's capabilities. Check with your Module's vendor manual whether USB3 supports OTG.

Please note that dual role devices should have a VBUS capacitance that is in a range of 1.0µF to 6.5µF.

The ESD diodes should be placed as close as possible to the connector. Take care that VBUS and ID pins are also protected against ESD events as they are directly connected to the SMARC 2.0 Module. The Module will control the power switch by driving USB3_EN_OC#. It will be driven low in order to cut-off power to VBUS as it is required for client mode.

Figure 18: USB3.2 OTG



2.6.7.2 EMI / ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins.

Common mode chokes can provide required noise attenuation but they also distort the signal quality of FullSpeed, HighSpeed and SuperSpeed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the Carrier Board design.

To protect the USB host interface of the Module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), low capacitance steering diodes and transient voltage suppression diodes have to be implemented on the Carrier Board design.

2.6.7.3 USB3.0/USB3.2 Differential Transitional Via Recommendations

Please refer to 2.2.4.1

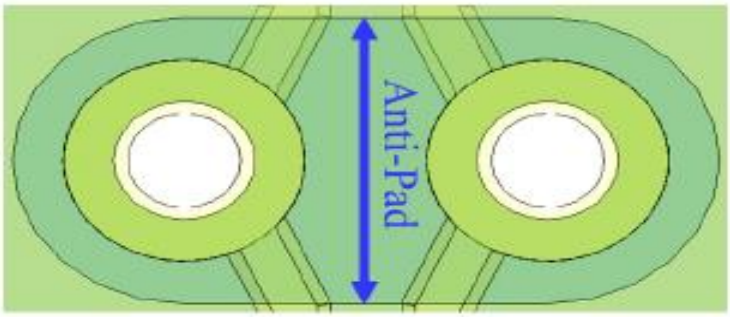
2.6.7.4 USB3.2 General Guidelines

• Trace Geometry: For Gen2, it is recommended to use 80-ohm trace geometry (with larger trace width), primarily to address routing insertion loss at 10Gbps. For Gen1, it is recommended to use 85-ohm trace geometry (narrower trace width), for PCB real estate saving. It is worth noting that Gen2 with 80-ohm trace geometry is fully functional and backward compatible with Gen1 5Gbps signaling.

• Reference plane: Continuous Ground.

• Via stub: For USB3.2 gen 2, via stub length < 15mils.

• Via anti-pad: Oval anti-pad size of 40mils is required for better impedance matching.



• AC capacitor value: 100nF nominal (75-265nF range).

• CMC: CMC is not needed for Rx lanes.

• ESD: ESD may/may not be required depending on the 3rd party's device. On the removal of discrete ESD, there are two requirements have to be met:
(a) Mux/Re-driver can handle the ESD at least 8kV
(b) Mux/Re-driver to be placed near to USB-C connector (< 1")
Refer to 3rd party component specification.

• Distance between coils should be greater than 12 mils (recommended is 15 mils).

2.6.8 USB3.2 Trace Length Guidelines

Figure 19: Topology for USB3.2

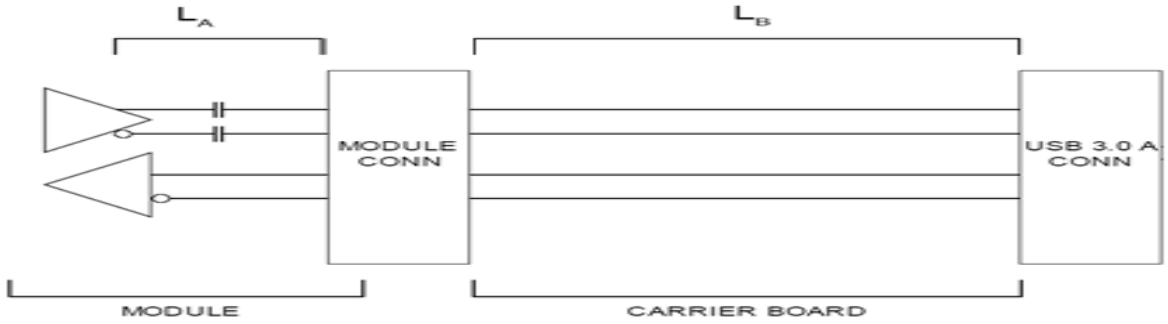


Table 21: USB3.2 Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	USB3.2	
Differential Impedance Target	Gen1: 85 Ω ±10% Gen2: 80 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	Gen1: 8.9” Gen2: 4.9”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. 2 vias per differential signal trace	

Notes:

2.7 SDIO Interface

The SD Card / SDIO interface can support SD Cards or additionally SDIO functionality. A SDIO (Secure Digital Input Output) card is an extension of the SD specification to cover I/O functions. SDIO cards are only fully functional in host devices designed to support their input-output functions. These devices can use the SD slot to support GPS receivers, modems, barcode readers, radio tuners, RFID readers, digital cameras, and interfaces to Wi-Fi, Bluetooth, Ethernet, and IrDA.

The SDIO and SD interfaces are mechanically and electrically identical. Host devices built for SDIO cards generally accept SD memory cards without I/O functions. However, the reverse is not true, because host devices need suitable drivers and applications to support the card's I/O functions.

2.7.1 SDIO Signal Definitions

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card flash memories.

Table 22: Signal Definition SDIO

Signal	Pin#	Description	I/O	Notes
SDIO_CD#	P35	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present. This signal has no pull up to 3.3V on the module. Carrier Board: Connect to CD# of SDIO/MMC device or card N/C if not used	I OD CMOS Runtime 1.8V or 3.3V	
SDIO_CK	P36	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz Carrier Board: Connect 10Ω near to SDIO connector. Connect to CLK of SDIO/MMC device or card N/C if not used	O CMOS Runtime 1.8V or 3.3V	1
SDIO_CMD	P34	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode. Carrier Board: Connect 10Ω near to SDIO connector. Connect to CMD of SDIO/MMC device or card N/C if not used	I/O CMOS Runtime 1.8V or 3.3V	1

Signal	Pin#	Description	I/O	Notes
SDIO_WP	P33	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards. This signal has no pull up to 3.3V on the module. Carrier Board: Connect to WP of SDIO/MMC device or card N/C if not used	I OD CMOS Runtime 1.8V or 3.3V	
SDIO_PWR_EN	P37	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device. Carrier Board: Connect to power enable of power distribution switch (with short circuit and thermal protection) N/C if not used	O CMOS Runtime 3.3V	
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3	P39 P40 P41 P42	SDIO Data lines. These signals operate in push-pull mode. Carrier Board: Connect 10Ω near to SDIO connector. Connect to DATA0-3 of SDIO/MMC device or card N/C if not used	I/O CMOS Runtime 1.8V or 3.3V	1

Note:

1. SDIO controller will detect SD Cards voltage level (1.8V for UHS-I and 3.3V for standard) and adjust its I/O voltage level accordingly.

2.7.2 SDIO Interface Routing Guidelines

Figure 20: Topology for SDIO

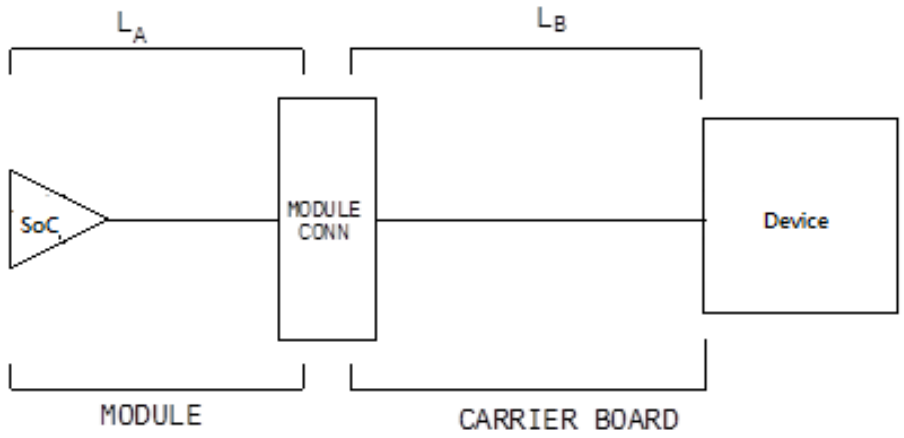


Table 23: SDIO Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SDIO	
Single End	50Ω ±10%	
DATA to CLK Maximum Pin to Pin Length Mismatch	200 mils	
Main Route segment for CMD/Data/CD#	Minimum Trace Spacing Between Other SD Card and Interface Signals 15 mils	
Main Route segment for CLK)	Minimum Trace Spacing Between Other SD Card and Interface Signals 15mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	7.9”	
Length matching	Data to Clock must be matched within ±25mils	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

Notes:

2.8 Audio HDA / I2S

Two audio interfaces are defined. One is pin shared with HDA, I2S1 from SMARC V1.1 has been deprecated.
The I2S interface is typically used for ARM processor implementation. HDA is typically used for x86 processor implementations. The HDA interface can also be used for a second I2S interface.

The HDA interface uses the same pins as I2S2 in SMARC 2.11 specification. At the time of writing HDA is still the preferred Audio Interface for x86 based Modules, even though I2S is getting integrated in the latest x86 SoC generations. There's a minor conflict with regards to voltage levels of the shared HDA and I2S audio interfaces. SMARC defines the I/O levels of HDA to be 1.5V to comply with the HDA specification. Nevertheless, there's a trend to run the HDA interface at 1.8V in order to save cost for additional voltage regulators. Most of chip vendors as well as codec vendors allow either voltage to be used. Please check with your Module vendor if 1.5V or 1.8V are supported and use an audio codec that is capable to support the regarding I/O voltage.

I2S Interfaces General Information:
The I2S (Inter IC Sound) bus specification was initially released in 1986 by Philips (NXP) and later revised in 1996. I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC Module can generally be configured as I2S master or slave. SMARC Modules may support up to three independent I2S interfaces each having separate input and output data lines.

2.8.1 HDA / I2S Signal Descriptions

2.8.1.1 I2S Signal Descriptions

Two I2S interfaces are defined. These are typically used for digital audio I/O and other modest bandwidth functions. A common audio master clock signal is also defined.

Table 24: I2S Signal Descriptions

Signal	Pin#	Description	I/O	Note
I2S0_LRCK	S39	Left& Right audio synchronization clock. Carrier Board: Audio - Connect to Audio CODEC pin LRCK M.2 - Connect to M.2 CONN pin I2S_WS	I/O CMOS Runtime 1.8V	
I2S0_SDOUT	S40	Digital audio Output. Carrier Board: Audio - Connect to Audio CODEC pin DIN M.2 - Connect to M.2 CONN pin I2S_SDO	O CMOS Runtime 1.8V	
I2S0_SDIN	S41	Digital audio Input. Carrier Board: Audio - Connect to Audio CODEC pin DOUT M.2 - Connect to M.2 CONN pin I2S_SDI	I CMOS Runtime 1.8V	
I2S0_CK	S42	Digital audio clock. Carrier Board: Audio - Connect 20 Ω in series to Audio CODEC pin BCLK M.2 - Connect to M.2 CONN pin I2S_SCK	I/O CMOS Runtime 1.8V	
AUDIO_MCK	S38	Master clock output to Audio codecs. Carrier Board: Audio - Connect 20 Ω in series to Audio CODEC pin MCLK	O CMOS Runtime 1.8V	

2.8.1.2 HDA / I2S Signal Descriptions

Table 25: HDA/I2S Signal Descriptions

Signal	Pin#	Description	I/O	Note
HDA_RST# / GPIO4	P112	HDA reset output (by means of GPIO4) Carrier Board: HDA - Connect 0 Ω in series to HDA CODEC pin RESET#	O CMOS Runtime 1.8V / 1.5V	1
HDA_SYNC / I2S2_LRCK	S50	I2S2 Left& Right audio synchronization clock / HDA sync Alternative use: I2S2_LRCK Carrier Board: HDA - Connect 0 Ω in series to HDA CODEC pin SYNC I2S - Connect to I2S Audio CODEC pin LRCK	I/O CMOS Runtime HDA : 1.8V/1.5V I2S2: 1.8V	1
HDA_SDO / I2S2_SDOUT	S51	I2S Digital audio Output / High Definition Audio data out Alternative use: I2S2_SDOUT Carrier Board: HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to HDA CODEC pin SDATA_IN I2S - Connect to I2S Audio CODEC pin DIN	O CMOS Runtime HDA : 1.8V/1.5V I2S2: 1.8V	1
HDA_SDI / I2S2_SDIN	S52	I2S Digital audio Input / High Definition Audio data in Alternative use: I2S2_SDI Carrier Board: HDA - Connect 33-47 Ω in series and PD 10KΩ(NL) to HDA CODEC pin SDATA_OUT I2S - Connect to I2S Audio CODEC pin DOUT	HDA : I/O CMOS Runtime 1.8V/1.5V I2S2: I CMOS Runtime 1.8V	1
HDA_CK / I2S2_CK	S53	I2S Digital audio clock/ High Definition Audio clock Alternative use: I2S2_CK Carrier Board: HDA - Connect 0 Ω in series to HDA CODEC pin BIT_CLK I2S - Connect 20 Ω in series to I2S Audio CODEC pin BCLK	HDA : O CMOS Runtime 1.8V/1.5V I2S2: I/O CMOS Runtime 1.8V	1

Note:

1. SOM-2532 is only support HDA.

2.8.2 Audio Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies and analog ground planes from the rest of the Carrier Board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:
Traces must be routed with a target impedance of 50Ω with an allowed tolerance of ±15%.
Ground return paths for the analog signals must be given special consideration.
Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines.
Locate the analog and digital signals as far as possible from each other.
Partition the Carrier Board with all analog components grouped together in one area and all digital components in another.
Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between the planes must be a minimum of 0.05 inch wide.
Route analog power and signal traces over the analog ground plane.
Route digital power and signal traces over the digital ground plane.
Position the bypassing and decoupling capacitors close to the IC pins with wide traces to reduce impedance.
Place the crystal or oscillator (depending on the codec used) as close as possible to the codec. (HDA implementations generally do not require a crystal at the codec)
Do not completely isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be a minimum of 0.05 inch wide.
Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. That is, no signal should cross the split/gap between the ground planes, because this would cause a ground loop, which in turn would greatly increase EMI emissions and degrade the analog and digital signal quality.

2.8.3 HDA / I2S Trace Length Guidelines

2.8.3.1 HDA Trace Length Guidelines

Figure 21: Topology for HDA

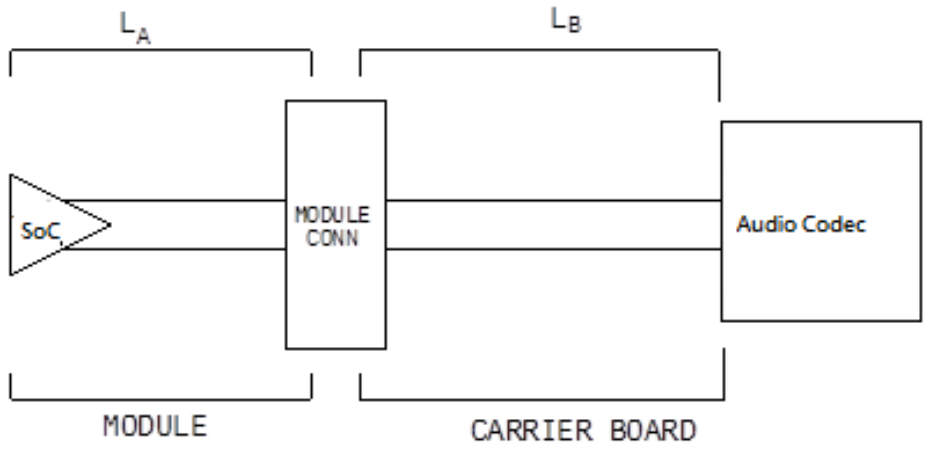


Table 26: HDA Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	HDA	
Single End	50Ω ±15%	
Nominal Trace Space within HDA Signal Group	Min. 15mils	
Spacing to Other Signal Group	Min. 20mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	14.4”	
Length matching	Data to Clock must be matched within ±125mils	
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	

Notes:

2.8.3.2 I2S Trace Length Guidelines

Figure 22: Topology for I2S

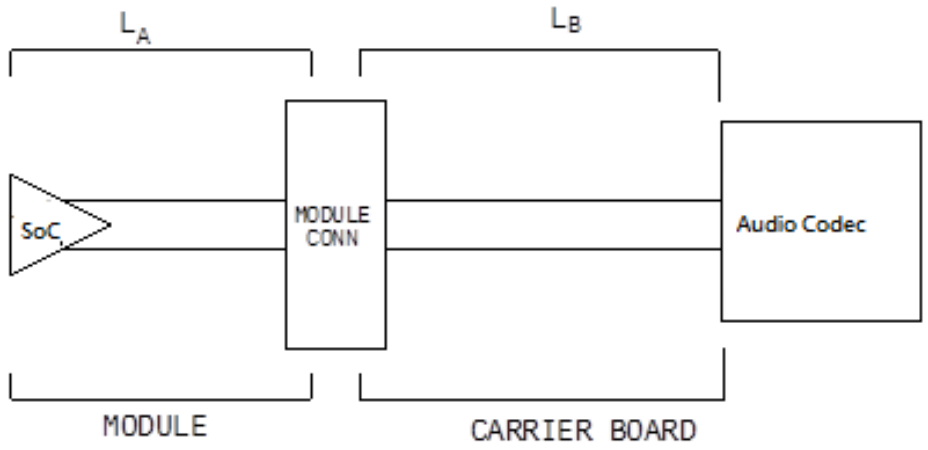


Table 27: I2S Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	I2S	1
Single End	50Ω ±15%	1
Nominal Trace Space within I2S Signal Group	Min. 15mils	1
Spacing to Other Signal Group	Min. 20mils	1
LA	NA	1
LB	Carrier Board Length	1
Max length of LA+LB	15”	1
Length matching	Data to Clock must be matched within 500mils	1
Reference Plane	GND referencing preferred. Min 20-mil trace edge-to-major plane edge spacing.	1

Notes:

1.SOM-2532 is not supported I2S2 for Audio.

2.9 LVDS

Single channel, dual channel or two single channel LVDS display panel interfaces are defined. The implementation of two single channel LVDS display interfaces is not expected to be common but is defined as an option for Advantech. The LVDS interfaces support 18 and 24 bit display implementations. Alternatively, the SMARC LVDS pins may also be used to implement eDP or MIPI DSI display interfaces. See Sections 2.9.1.1 LVDS / eDP Pin Sharing and 2.10.1.1 LVDS / DSI Pin Sharing below. In a Module implementation with two single LVDS channels, the panel EDID proms would be in conflict and measures need to be taken to avoid this. One possible solution is that the 2nd LVDS EDID prom could be read over the I2C_GP pin pair rather than the I2C_LCD pin pair.

The Module should implement an 18 / 24 bit dual channel LVDS output stream for the Primary display. This stream is usually created from the parallel RGB data, and usually carries the same display information, but in the serialized LVDS format. Control data (HS, VS, DE) are included in the LVDS stream.

All 18 bit TFT panels use the same LVDS color mapping. Only 3 data pairs (LVDS[0:1]_[0:2] +/-) and the clock pair are needed to drive an 18 bit TFT panel.
Unfortunately, there are two 24 bit LVDS color mappings in the industry:

Most significant color bits on the 4th LVDS data pair (LVDS[0:1]_[3] +/- here). This is the more common 24 bit mapping. It is not compatible with the 18 bit LVDS color mapping.

Least significant color bits on the 4th LVDS data pair. This is compatible with the 18 LVDS color mapping.

Modules that implement LVDS shall implement single channel 18 bit LVDS; should implement a 24 bit “18 bit compatible” LVDS mapping and may implement the “MS bit on 4th LVDS pair” mapping. The second LVDS channel may be implemented.

2.9.1 Signal Definitions

Table 28: LVDS Signal Definitions

Signal	Pin#	Description	I/O	Note
LVDS1_0+ LVDS1_0-	S111 S112	LVDS channel 1 differential signal pair 0 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXinO0+/- with 100Ω termination Conn. - RXinO0+/- N/C if not used	O LVDS Runtime	1,4
LVDS1_1+ LVDS1_1-	S114 S115	LVDS channel 1 differential signal pair 1 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO1+/- with 100Ω termination Conn. – RxinO1+/- N/C if not used	O LVDS Runtime	1,4
LVDS1_2+ LVDS1_2-	S117 S118	LVDS channel 1 differential signal pair 2 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO2+/- with 100Ω termination Conn. – RxinO2+/- N/C if not used	O LVDS Runtime	1,4
LVDS1_3+ LVDS1_3-	S120 S121	LVDS channel 1 differential signal pair 3 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinO3+/- with 100Ω termination Conn. – RxinO3+/- N/C if not used	O LVDS Runtime	1,4
LVDS1_CK+ LVDS1_CK-	S108 S109	LVDS channel 1 differential clock pair Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXOC+/- with 100Ω termination Conn. - RXOC+/- N/C if not use	O LVDS Runtime	1,4

Signal	Pin#	Description	I/O	Note
LVDS0_0+ LVDS0_0-	S125 S126	LVDS channel 0 differential signal pair 0 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXinE0+/- with 100Ω termination Conn. - RXinE0+/- N/C if not used	O LVDS Runtime	1,5
LVDS0_1+ LVDS0_1-	S128 S129	LVDS channel 0 differential signal pair 1 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE1+/- with 100Ω termination Conn. – RxinE1+/- N/C if not used	O LVDS Runtime	1,5
LVDS0_2+ LVDS0_2-	S131 S132	LVDS channel 0 differential signal pair 2 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE2+/- with 100Ω termination Conn. – RxinE2+/- N/C if not used	O LVDS Runtime	1,5
LVDS0_3+ LVDS0_3-	S137 S138	LVDS channel 0 differential signal pair 3 Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever – RxinE3+/- with 100Ω termination Conn. – RxinE3+/- N/C if not used	O LVDS Runtime	1,5
LVDS0_CK+ LVDS0_CK-	S134 S135	LVDS channel 0 differential clock pair Carrier Board: Connect 100Ω @100MHz Common Choke in series to Reciever - RXEC+/- with 100Ω termination Conn. - RXEC+/- N/C if not used	O LVDS Runtime	1,5
LCD1_VDD_EN LCD0_VDD_EN	S116 S133	High enables panel VDD . Carrier Board: Connect to enable control of LVDS panel power circuit. N/C if not used	O CMOS Runtime 1.8V	2

Signal	Pin#	Description	I/O	Note
LCD1_BKLT_EN LCD0_BKLT_EN	S107 S127	LVDS flat panel backlight enable high active signal Carrier Board: Connect to enable control of LVDS panel backlight power circuit. N/C if not used	O CMOS Runtime 1.8V	2
LCD1_BKLT_PWM LCD0_BKLT_PWM	S122 S141	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this purpose it can be used as General Purpose PWM Output. Carrier Board: Connect to brightness control of LVDS panel backlight power circuit. N/C if not used	O CMOS Runtime 1.8V	2
I2C_LCD_DAT	S140	I2C data – to read LCD display EDID EEPROMs Be aware of possible EDID PROM address conflicts if multiple displays are implemented This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to DDC data of LVDS panel N/C if not used	I/O OD CMOS Runtime 1.8V	3
I2C_LCD_CK	S139	I2C clock – to read LCD display EDID EEPROMs. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to DDC clock of LVDS panel N/C if not used	I/O OD CMOS Runtime 1.8V	3

Note:

1. 100 ohm differential termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.
2. Only in use, when two separate LVDS ports are supported, please check Advantech Module user manual.
3. Possible conflict if two LVDS panels are used.
4. LVDS1 only. If eDP0 or DSI0 function is used, LVDS1 will be no function.
5. Default LVDS0, eDP0 or DSI0 is option function.

2.9.1.1 Display Timing Configuration

The graphic controller needs to be configured to match the timing parameters of the attached flat panel display. To properly configure the controller, there needs to be some method to determine the display parameters. Different Module vendors provide differing ways to access display timing parameters. Some vendors store the data in non-volatile memory with the BIOS setup screen as the method for entering the data, other vendors might use a Module or Carrier based EEPROM. Some vendors might hard code the information into the BIOS, and other vendors might support panel located timing via the signals LVDS_I2C_CLK and LVDS_I2C_DAT with an EEPROM strapped to 1010 000x. Regardless of the method used to store the panel timing parameters, the video BIOS will need to have the ability to access and decode the parameters. Given the number of variables it is recommended that Carrier designers contact Module suppliers to determine the recommend method to store and retrieve the display timing parameters.

The Video Electronics Standards Association (VESA) recently released DisplayID, a second generation display identification standard that can replace EDID and other proprietary methods for storing flat panel timing data. DisplayID defines a data structure which contains information such as display model, identification information, colorimetry, feature support, and supported timings and formats. The DisplayID data allows the video controller to be configured for optimal support for the attached display without user intervention. The basic data structure is a variable length block up to 256 bytes with additional 256 byte extensions as required. The DisplayID data is typically stored in a serial EPROM connected to the LVDS_I2C bus. The EPROM can reside on the display or Carrier. DisplayID is not backwards compatible with EDID. Contact VESA (www.vesa.org) for more information.

2.9.1.2 Backlight Control

Backlight inverters are either voltage, PWM or resistor controlled. The SMACR specification provides one method for controlling the brightness. One method is to use the backlight control and enable signals from the CPU chipset. These signals are brought on SMARC LCD_BKLT_EN and LCD_BKLT_PWM. LCD_BKLT_PWM is a Pulse Width Modulated (PWM) output that can be connected to display inverters that accept a PWM input.

2.9.2 LVDS Routing Guidelines

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100Ω or 85Ω differential impedance and a 50-Ω, single-ended impedance. Ideally, a LVDS pair is routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. Reference LVDS pairs to a power plane if necessary. The power plane should be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is required. Intra-pair matching is tighter than the inter-pair matching.

All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly.

2.9.3 LVDS Trace Length Guidelines

Figure 23: Topology for LVDS

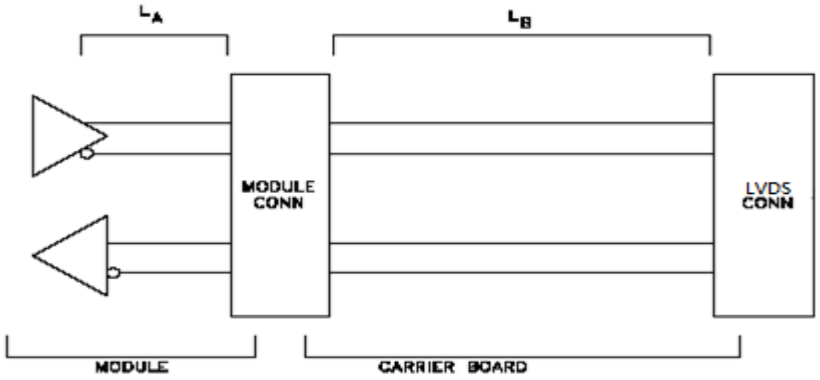


Table 29: LVDS Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	LVDS	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Signal length to the LVDS connector available for the SMARC Carrier Board	4”	
Spacing between pair to pairs (inter-pair) (s)	Min. 20 mils	
Spacing between differential pairs and high-speed periodic signals	Min. 30 mils	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	4”	
Length matching	Differential pairs (intra-pair): Max. ±5 mils Clock and data pairs (intra-pair): Max. ±100 mils data pairs (inter-pair) : Max. ±100 mils	
Reference Plane	GND referencing preferred	
Spacing from edge of plane	Min. 40mils	
Carrier Board Via Usage	Max. of 2 vias per line.	

Notes:

2.10 Embedded DisplayPort (eDP) *SOM-2532 is Option function

SMACR Rev 2.11 modules optionally support up to two Embedded DisplayPort (eDP) Version 1.2 interfaces. These interfaces are shared with LVDS signals.

eDP is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The eDP specification defines a scalable digital display interface. It defines a license-free, royalty-free, state-of-the-art digital video interconnect intended to be used primarily between a computer and its internal display(s). The eDP interface supports 1, 2, or 4 data pairs that carry the video signal and embeds the clock in the data signal. The eDP interface is designed to replace LVDS as an internal Graphics interface in the coming years. Benefits are embedded clock, higher data rates and less data lines than with LVDS. EDP support is offered by ARM and x86 processor based platforms, depending on the selected processor. DC blocking capacitors shall be placed on the Carrier board. If the eDP display interface of the SMARC module is not implemented, all signals associated with this interface should be left open.

2.10.1 eDP Signal Definitions

Table 30: eDP Signal Definitions

Signal	Pin#	Description	I/O	Note
eDP1_TX0+ eDP1_TX0-	S111 S112	eDP1 lane 0, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	1,4
eDP1_TX1+ eDP1_TX1-	S114 S115	eDP1 lane 1, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	1,4
eDP1_TX2+ eDP1_TX2-	S117 S118	eDP1 lane 2, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	1,4

Signal	Pin#	Description	I/O	Note
eDP1_TX3+ eDP1_TX3-	S120 S121	eDP1 lane 3, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	1,4
eDP1_AUX+ eDP1_AUX-	S108 S109	eDP1 auxiliary lane +/- Carrier Board: Connect to device or eDP connector. N/C if not used.	I/O DP Runtime	1,4
eDP1_HPD	S113	eDP1 Detection of Hot Plug / Unplug and notification of the link layer Carrier Board: Connector to device or eDP connector HP pin.	I CMOS Runtime 1.8V	1, NC pin
eDP0_TX0+ eDP0_TX0-	S125 S126	eDP0 lane 0, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	5
eDP0_TX1+ eDP0_TX1-	S128 S129	eDP0 lane 1, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	5
eDP0_TX2+ eDP0_TX2-	S131 S132	eDP0 lane 2, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	5
eDP0_TX3+ eDP0_TX3-	S137 S138	eDP0 lane 3, TX +/- Carrier Board: DC blocking capacitors shall be placed on the Carrier board. Connect to device or eDP connector. N/C if not used	O DP Runtime	5

Signal	Pin#	Description	I/O	Note
eDP0_AUX+ eDP0_AUX-	S134 S135	eDP0 auxiliary lane +/- Carrier Board: Connect to device or eDP connector. N/C if not used.	I/O DP Runtime	5
eDP0_HPD	S144	eDP0 Detection of Hot Plug / Unplug and notification of the link layer Carrier Board: Connector to device or eDP connector HP pin.	I CMOS Runtime 1.8V	5
LCD1_VDD_EN LCD0_VDD_EN	S116 S133	High enables panel VDD . eDP 0/1 VDD_EN support over EDP_AUX channel is preferable. Carrier Board: Connect to enable control of LVDS panel power circuit. N/C if not used	O CMOS Runtime 1.8V	1
LCD1_BKLT_EN LCD0_BKLT_EN	S107 S127	LVDS flat panel backlight enable high active signal. eDP 0/1 BKLT_EN support over EDP_AUX channel is preferable. Carrier Board: Connect to enable control of LVDS panel backlight power circuit. N/C if not used	O CMOS Runtime 1.8V	1
LCD1_BKLT_PWM LCD0_BKLT_PWM	S122 S141	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this purpose it can be used as General Purpose PWM Output. eDP 0/1 BLK_PWM support over EDP_AUX channel is preferable. Carrier Board: Connect to brightness control of LVDS panel backlight power circuit. N/C if not used	O CMOS Runtime 1.8V	1
I2C_LCD_DAT	S140	I2C data – to read LCD display EDID EEPROMs Be aware of possible EDID PROM address conflicts if multiple displays are implemented. Optional - eDP panel information is usually obtained over the eDP AUX pair. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to DDC data of LVDS panel N/C if not used	I/O OD CMOS Runtime 1.8V	2

Signal	Pin#	Description	I/O	Note
I2C_LCD_CK	S139	I2C clock – to read LCD display EDID EEPROMs. Optional - eDP panel information is usually obtained over the eDP AUX pair. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to DDC clock of LVDS panel N/C if not used	I/O OD CMOS Runtime 1.8V	3

Notes:

1. When two separated eDP ports are supported. Please check Advantech Module user manual.
2. Possible EDID EEPROM Address conflicts may occur if multiple displays are implemented.
   Optional - eDP panel information is usually exchanged via the eDP auxiliary pair.
3. Optional - eDP panel information is usually exchanged via the eDP auxiliary pair.
4. SOM-2532 is no support eDP1 and DSI1.
5. Default LVDS0, eDP0 or DSI0 is option function.

2.10.1.1 LVDS / eDP Pin Sharing

Pins used for LVDS LCD support *may* alternatively be used to support up to two Embedded DisplayPorts.

The AC coupling required for eDP operation *shall* be done off-Module.

Table 31: LVDS / eDP Pin Sharing

LVDS Pin Pairs	LCD Support Pins / Other Pins	eDP Usage	Notes
LVDS0_0+ LVDS0_0-		eDP0_TX0+ eDP0_TX0-	eDP0 data pair 0
LVDS0_1+ LVDS0_1-		eDP0_TX1+ eDP0_TX1-	eDP0 data pair 1
LVDS0_2+ LVDS0_2-		eDP0_TX2+ eDP0_TX2-	eDP0 data pair 2
LVDS0_3+ LVDS0_3-		eDP0_TX3+ eDP0_TX3-	eDP0 data pair 3
LVDS0_CK+ LVDS0_CK-		eDP0_AUX+ eDP0_AUX-	eDP0 auxiliary channel pair
LVDS1_0+ LVDS1_0-		eDP1_TX0+ eDP1_TX0-	eDP1 data pair 0
LVDS1_1+ LVDS1_1-		eDP1_TX1+ eDP1_TX1-	eDP1 data pair 1
LVDS1_2+ LVDS1_2-		eDP1_TX2+ eDP1_TX2-	eDP1 data pair 2
LVDS1_3+ LVDS1_3-		eDP1_TX3+ eDP1_TX3-	eDP1 data pair 3
LVDS1_CK+ LVDS1_CK-		eDP1_AUX+ eDP1_AUX-	eDP1 auxiliary channel pair
	I2C_LCD_CK I2C_LCD_DAT		Optional - eDP panel information is usually obtained over the eDP AUX pair
	LCD[0:1]_VDD_EN	LCD[0:1]_VDD_EN	eDP 0/1 VDD_EN support over EDP_AUX channel is preferable
	LCD[0:1]_BKLT_EN	LCD[0:1]_BKLT_EN	eDP 0/1 BKLT_EN support over EDP_AUX channel is preferable
	LCD[0:1]_BKLT_PWM	LCD[0:1]_BKLT_PWM	eDP 0/1 BKLT_PWM support over EDP_AUX channel is preferable
		EDP[0:1]_HPD	eDP 0/1Hot Plug Detect pins

2.10.2 eDP Implementation Guidelines

Many carrier board designs do not need the full range of eDP performance offered by SMARC modules. It depends on the flat panel configuration of the SMARC module, as well as the carrier board design, as to how many eDP lanes are supported. In this case all unused eDP signal lanes should be left open on the carrier board. If the eDP display interface of the SMARC module is not implemented at all, non-shared signals associated with this interface should be left open.

2.10.3 eDP Trace Length Guidelines

Figure 24: Topology for eDP

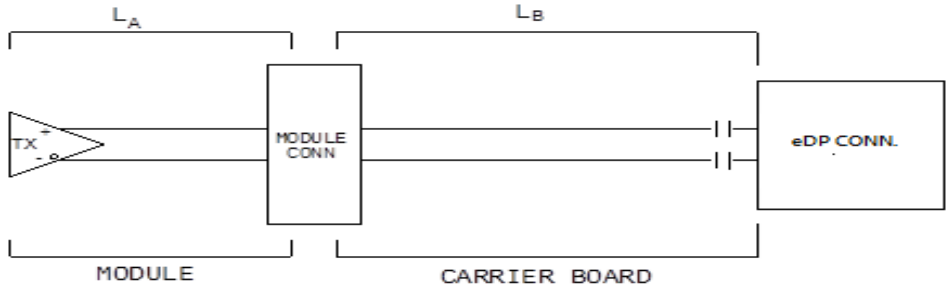


Table 32: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	eDP	1
Differential Impedance Target	85 Ω ±10%	1
Single End	50Ω ±10%	1
Isolation to equivalent pairs	15 mils (MS) and 15 mils (DS)	1
Isolation to other signal groups	15 mils (MS) and 15 mils (DS)	1
LA	Please see the SOM-2532 Layout Checklist	1
LB	Carrier Board Length	1
Max length of LA+LB	eDP differential pairs to eDP connector: 10” AUX channel: 10”	1
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 1-inch window (max length – min length < 1 inch (2.54 cm)).	1
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	1
Carrier Board Via Usage	Max. 3 vias.	1

Notes:

1. SOM-2532 default is not supported eDP, it is option function. If customers want to use eDP function, please contact Advantech.

2.11 MIPI DSI *SOM-2532 is Option function.

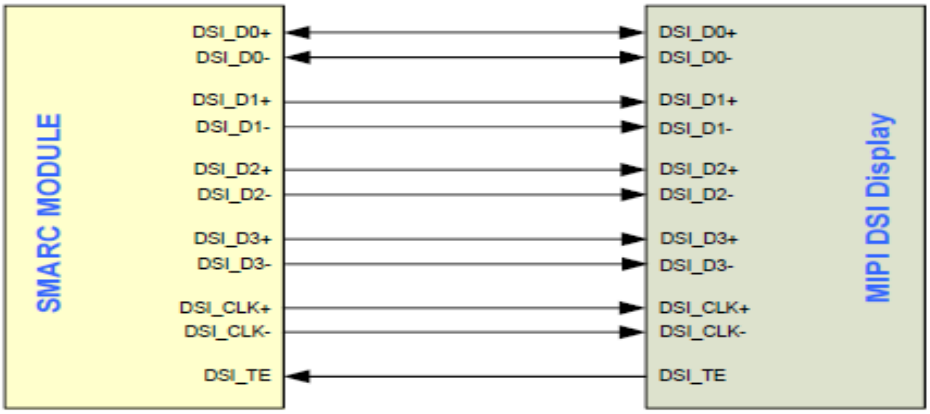
The LVDS signal lines may alternatively be used to support up to two MIPI DSI (Display Serial Interface) displays. DSI is a high-speed differential bus and includes one clock lane and up to four data lanes.

There is no AC coupling required.

VDD and Backlight signals are the same is in LVDS mode.

It is recommended to check with Advantech if MIPI DSI is supported by the used SMARC Module.

Figure 25: MIPI DSI



2.11.1 DSI Signal Definitions

Table 33: DSI Signal Definitions

Signal	Pin#	Description	I/O	Note
DSI1_D0+ DSI1_D0-	S111 S112	MIPI DSI1 data lane 0, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI1_D1+ DSI1_D1-	S114 S115	MIPI DSI1 data lane 1, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI1_D2+ DSI1_D2-	S117 S118	MIPI DSI1 data lane 2, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1

Signal	Pin#	Description	I/O	Note
DSI1_D3+ DSI1_D3-	S120 S121	MIPI DSI1 data lane 3, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI1_CLK+ DSI1_CLK-	S108 S109	MIPI DSI1 clock. Carrier Board: Connect to device or DSI connector. N/C if not used.	O D-PHY Runtime	1
eDP1_HPD / DSI1_TE (For SMARC2.1 only)	S113	DSI1 tearing effect signal Carrier Board: Connect to device or DSI connector.	I CMOS Runtime 1.8V	NC ping
DSI0_D0+ DSI0_D0-	S125 S126	MIPI DSI0 data lane 0, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI0_D1+ DSI0_D1-	S128 S129	MIPI DSI0 data lane 1, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI0_D2+ DSI0_D2-	S131 S132	MIPI DSI0 data lane 2, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI0_D3+ DSI0_D3-	S137 S138	MIPI DSI0 data lane 3, D +/- Carrier Board: No blocking capacitors or termination required. Connect to device or DSI connector. N/C if not used	O D-PHY Runtime	1
DSI0_CLK+ DSI0_CLK-	S134 S135	MIPI DSI0 clock. Carrier Board: Connect to device or DSI connector.. N/C if not used.	O D-PHY Runtime	1

Signal	Pin#	Description	I/O	Note
eDP0_HPD / DSI0_TE(For SMARC2.1 only)	S144	DSI0 tearing effect signal Carrier Board: Connect to device or DSI connector.	I CMOS Runtime 1.8V	1

Notes:

1. Default LVDS0, eDP0 or DSI0 is option function. SOM-2532 only support x4 lanes.

2.11.1.1 LVDS / DSI Pin Sharing

Pins used for LVDS LCD support *may* alternatively be used to support a MIPI DSI (Display Serial Interface). There is no AC coupling required for DSI operation.

Table 34: LVDS / DSI Pin Sharing

LVDS Pin Pairs	LCD Support Pins / Other Pins	DSI Usage	Notes
LVDS0_0+ LVDS0_0-		DSI0_D0+ DSI0_D0-	DSI0 data pair 0
LVDS0_1+ LVDS0_1-		DSI0_D1+ DSI0_D1-	DSI0 data pair 1
LVDS0_2+ LVDS0_2-		DSI0_D2+ DSI0_D2-	DSI0 data pair 2
LVDS0_3+ LVDS0_3-		DSI0_D3+ DSI0_D3-	DSI0 data pair 3
LVDS0_CK+ LVDS0_CK-		DSI0_CLK+ DSI0_CLK-	DSI0 clock pair
LVDS1_0+ LVDS1_0-		DSI1_D0+ DSI1_D0-	DSI1 data pair 0
LVDS1_1+ LVDS1_1-		DSI1_D1+ DSI1_D1-	DSI1 data pair 1
LVDS1_2+ LVDS1_2-		DSI1_D2+ DSI1_D2-	DSI1 data pair 2
LVDS1_3+ LVDS1_3-		DSI1_D3+ DSI1_D3-	DSI1 data pair 3
LVDS1_CK+ LVDS1_CK-		DSI1_CLK+ DSI1_CLK-	DSI1 clock pair
	I2C_LCD_CK I2C_LCD_DAT		
	LCD[0:1]_VDD_EN	LCD[0:1]_VDD_EN	
	LCD[0:1]_BKLT_EN	LCD[0:1]_BKLT_EN	
	LCD[0:1]_BKLT_PWM	LCD[0:1]_BKLT_PWM	
	EDP[0:1]_HPD	DSI[0:1]_TE	DSI 0/1 tearing effect signal

2.11.2 DSI Topology Guidelines

The following figure and table illustrates the routing topology and length guidelines for the differential signals (DATA and CLK).

2.11.3 DSI Trace Length Guidelines

Figure 26: Topology for DSI

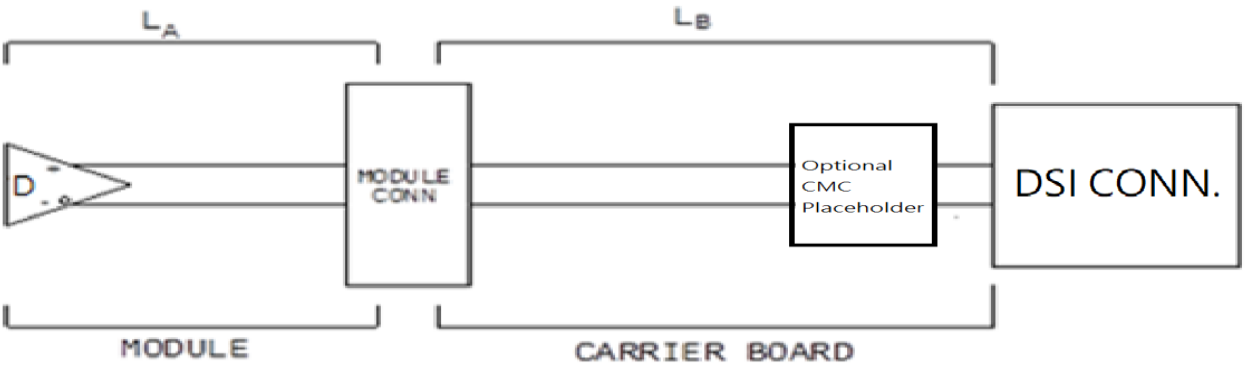


Table 35: DSI Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	DSI	
Differential Impedance Target	100 Ω ±10%	
Single End	50Ω ±10%	
Isolation to equivalent pairs	15 mils (MS) and 15 mils (DS)	
Isolation to other signal groups	15 mils (MS) and 15 mils (DS)	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DSI differential pairs to DSI connector: Link Rate: <= 1.0Gbps 19” Link Rate: <= 1.5Gbps 19” Link Rate: <= 2.0Gbps 14.9” Link Rate: <= 2.5Gbps 14.9”	
Length matching	Length Matching between P and N within a diff. pair: Max. ±2.5 mils Length Matching between Data and Clock: . Max. ±40 mils	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 3 vias.	

Notes:

2.12 DisplayPort(DP) / HDMI Interfaces *SOM-2532 is Option function.

2.12.1 DisplayPort / HDMI Interface Signals (from Module)

SMACR Rev 2.11 modules optionally support one DisplayPort interface. This interface is shared with HDMI signals.

DisplayPort is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

The DisplayPort interface supports 1, 2, or 4 data pairs that carry the video signal, clock and optional audio signals. The video signal of the DisplayPort interface is not compatible with HDMI but a DisplayPort connector can pass these signals through. While HDMI requires separate clock signals, DisplayPort embeds the clock in the data signal. Unlike the separate HDMI and LVDS standards, DisplayPort supports both external (monitor) or internal (LCD panel) display connections.

Display Port++ (also known as dual-mode DisplayPort) output signals can easily provide the lower voltages required for Display Port using a passive adapter. This enables cost-efficient direct support for single-link HDMI signals. Dual-mode chipsets are able to detect when a HDMI passive adapter is connected and then switch to HDMI mode using the 4-lane main DisplayPort link and the AUX channel link to transmit 3 HDMI signals, clock and display data channel Data and Clock. Dual-mode compatible devices are recognizable by the DP++ logo.

Note:

1. *AC coupling is provided on the carrier board for the main link, auxiliary channel needs AC coupling on the module.*
2. *HDMI displays uses 5V I2C signaling. The Module HDMI_CTRL_DAT and HDMI_CTRL_CK signals need to be level translated on the Carrier from the Module 1.8V level. A similar consideration applies to the HDMI_HPD signal. There are a number of single chip devices on the market that perform ESD protection and control signal level shifting for HDMI interfaces.*
3. *Dual Mode (HDMI and DisplayPort on the same pins) implementations may be realized. This is desirable for SOCs that natively implement this capability. With such SOCs, the primary Dual Mode implementation challenge is that the HDMI_CTRL_DAT and HDMI_CTRL_CK lines are DC coupled, but the DP_AUX+ /- pair must be AC coupled. A set of FET switches is usually used to sort this out. The FET gates can be controlled by the AUX_SEL pin function.*

Table 36: Signal Definition DisplayPort / HDMI

Signal	Shared With	Pin#	Description	I/O	Notes
HDMI_D2+ HDMI_D2-	DP1_LANE0+ DP1_LANE0-	P92 P93	HDMI data differential pairs DP Data Pair 0 Carrier Board: For HDMI Connector, connect to HDMI Conn pin 1 HDMI_D2+, pin 3 HDMI_D2- and ESD protection N/C if not used. For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 0(+), ML_Lane 0(-). DP Connector- Connect to DP Conn pin 1 ML_Lane 0(+), pin 3 ML_Lane 0(-) and ESD protection N/C if not used.	HDMI: O TMDS DP: O DP Runtime	3
HDMI_D1+ HDMI_D1-	DP1_LANE1+ DP1_LANE1-	P95 P96	HDMI data differential pairs DP Data Pair 1 Carrier Board: For HDMI Connector, connect to HDMI Conn pin 4 HDMI_D1+, pin 6 HDMI_D1- and ESD protection N/C if not used. For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 1(+), ML_Lane 1(-). DP Connector - Connect to DP Conn pin 4 ML_Lane 1(+), pin 6 ML_Lane 1(-) and ESD protection N/C if not used.	HDMI: O TMDS DP: O DP Runtime	3

Signal	Shared With	Pin#	Description	I/O	Notes
HDMI_D0+ HDMI_D0-	DP1_LANE2+ DP1_LANE2-	P98 P99	HDMI data differential pairs DP Data Pair 2 Carrier Board: For HDMI Connector, connect to HDMI Conn pin 7 HDMI_D0+, pin 9 HDMI_D0- and ESD protection N/C if not used. For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 2(+), ML_Lane 2(-). DP Connector - Connect to DP Conn pin 7 ML_Lane 2(+), pin 9 ML_Lane 2(-) and ESD protection N/C if not used.	HDMI: O TMDS DP: O DP Runtime	3
HDMI_CK+ HDMI_CK-	DP1_LANE3+ DP1_LANE3-	P101 P102	HDMI clock pairs DP Data Pair 3 Carrier Board: For HDMI Connector, connect to HDMI Conn pin 10 HDMI_CK+, pin 12 HDMI_CK- and ESD protection N/C if not used. For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 3(+), ML_Lane 3(-). DP Connector- Connect to DP Conn pin 10 ML_Lane 3(+), pin 12 ML_Lane 3(-) and ESD protection N/C if not used.	HDMI: O TMDS DP: O DP Runtime	3

Signal	Pin#	Description	I/O	Notes
HDMI_CTRL_CK HDMI_CTRL_DAT	P105 P106	I2C clock line dedicated to HDMI I2C data line dedicated to HDMI Carrier Board: Pull-ups to 1.8V on each of these lines is required on the Carrier. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device. If discrete Carrier pull-ups are used, they should be 10K or 100K pull-up to 1.8V. For HDMI Connector, connect to HDMI Conn pin 15 HDMI_CTRL_CK, pin 16 HDMI_CTRL_DAT and ESD protection N/C if not used.	CK: I/O OD CMOS 1.8V DAT: /O OD CMOS 1.8V Retime	1, 3
DP1_AUX+ DP1_AUX-	P105 P106	Auxiliary channel used for link management and device control. Differential pair lines. There are AC Coupled 0.1uF on module. DP1_AUX+ has pull-down 100K on module. DP1_AUX- has pull-up 100K on module. Carrier Board: Device - Connect to DP receiver AUX CH(+) and AUX CH(-). DP Connector - Connect to DP Conn pin 15 AUX CH(+) and ESD protection Connect to DP Conn pin 17 AUX CH(-) and ESD protection N/C if not used.	I/O DP Runtime 3.3V	2, 3
HDMI_HPD	P104	Hot plug detection signal that serves as an interrupt request. Module has integrated current blocking circuit or Logic inversion and PD 100K Ω resistor to GND. Carrier Board: Connect to HDMI Connector - HDMI Conn pin 19 Hot Plug Detect N/C if not used.	I COMS Runtime 1.8V	3

Signal	Pin#	Description	I/O	Notes
DP1_HPD	P104	Hot plug detection signal that serves as an interrupt request. Module has integrated current blocking circuit or Logic inversion and PD 100K Ω resistor to GND Carrier Board: The carrier shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the module. Device - Connect to DP device Hot Plug Detect DP Connector - Connect to DP Conn pin 18 Hot Plug Detect N/C if not used.	I COMS Runtime 1.8V	3
DP1_AUX_SEL	P107	Selects the function of DP1_AUX+ and DP1_AUX-. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the HDMI_CTRL_CK and HDMI_CTRL_DAT signals. Terminated on Module through 1M Ω resistor to GND. Carrier Board: Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI operation.	I COMS Runtime 1.8V	3

Notes:

1. Level shifter FET and 5V PU resistor shall be placed between the Module and the HDMI connector. Stronger pull-up is demanded to the carrier board. The pull-ups may be part of an integrated HDMI ESD protection and control-line level shift device.
   If discrete Carrier pull-ups are used, the value depends on the individual carrier board implementation.
2. If DP1_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP1_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
3. SOM-2532 DP is option function.

2.12.2 DP++

A DP++ interface can output signals that are formatted per either DP or HDMI / DVI protocols. The signal levels are DP compliant. For DP use, off-module coupling caps are needed on the 4 DP display data lanes. A Carrier Board level translator is usually needed for HDMI / DVI operation.

DP++ or DisplayPort++ (also named as Dual-mode DisplayPort) can directly output HDMI and DVI signals. The level adaptation can be implemented on the Carrier or via plug in cable adapter. In case of Carrier Board implementation a level shifter adjusts the I/O voltage to HDMI/DVI compliant signal levels. A dual-mode chipset switches to DVI/HDMI mode (4-lane main DisplayPort link and AUX channel) if a DVI or HDMI passive adapter is detected (by DP0_AUX_SEL).

Table 37: Signal Definition DP++

Signal	Pin#	Description	I/O	Notes
DP0_LANE0+ DP0_LANE0-	S93 S94	DP Data Pair 0 Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 0(+), ML_Lane 0(-). DP Connector- Connect to DP Conn pin 1 ML_Lane 0(+), pin 3 ML_Lane 0(-) and ESD protection N/C if not used.	I/O DP Runtime	
DP0_LANE1+ DP0_LANE1-	S96 S97	DP Data Pair 1 Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 1(+), ML_Lane 1(-). DP Connector - Connect to DP Conn pin 4 ML_Lane 1(+), pin 6 ML_Lane 1(-) and ESD protection N/C if not used.	I/O DP Runtime	
DP0_LANE2+ DP0_LANE2-	S99 S100	DP Data Pair 2 Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 2(+), ML_Lane 2(-). DP Connector - Connect to DP Conn pin 7 ML_Lane 2(+), pin 9 ML_Lane 2(-) and ESD protection N/C if not used.	I/O DP Runtime	

Signal	Pin#	Description	I/O	Notes
DP0_LANE3+ DP0_LANE3-	S102 S103	DP Data Pair 3 Carrier Board: For DP, connect AC Coupling Capacitors 75~200 nF near module to device or DP connector. Device - Connect to DP receiver ML_Lane 3(+), ML_Lane 3(-). DP Connector- Connect to DP Conn pin 10 ML_Lane 3(+), pin 12 ML_Lane 3(-) and ESD protection N/C if not used.	I/O DP Runtime	
DP0_AUX+ DP0_AUX-	S105 S106	Auxiliary channel used for link management and device control. Differential pair lines. There are AC Coupled 0.1uF on module. DP0_AUX+ has pull-down 100K Ω on module. DP0_AUX- has pull-up 100K Ω on module. Carrier Board: Device - Connect to DP receiver AUX CH(+) and AUX CH(-). DP Connector - Connect to DP Conn pin 15 AUX CH(+) and ESD protection Connect to DP Conn pin 17 AUX CH(-) and ESD protection N/C if not used.	I/O DP Runtime 3.3V	1
DP0_HPD	S98	Hot plug detection signal that serves as an interrupt request. Module has integrated current blocking circuit or Logic inversion and PD 100K Ω resistor to GND Carrier Board: The carrier shall include a blocking FET on DP1_HPD to prevent back-drive current from damaging the module. Device - Connect to DP device Hot Plug Detect DP Connector - Connect to DP Conn pin 18 Hot Plug Detect N/C if not used.	I COMS Runtime 1.8V	

Signal	Pin#	Description	I/O	Notes
DP0_AUX_SEL	S95	Selects the function of DP0_AUX+ and DP1_AUX-. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the HDMI_CTRL_CK and HDMI_CTRL_DAT signals. Terminated on Module through 1M Ω resistor to GND. Carrier Board: Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations. Driven to 1.8V on Carrier for HDMI operation.	I COMS Runtime 1.8V	2

Note:

1. If DP0_AUX_SEL=0 (DP mode): AC coupled on module, 100k PD. If DP0_AUX_SEL=1 (HDMI mode): DC coupled, CMOS, 100k PU. In case of HDMI over DP++ implementation, stronger pull-up is demanded to the Carrier Board.
2. Pulled to GND on Carrier for DP operation in Dual Mode (DP++) implementations Module must tolerate high level in stand-by mode. Should be connected to pin 13 of the DisplayPort connector to enable a dual-mode DisplayPort interface.

2.12.3 DisplayPort Interfaces Routing Guidelines

2.12.3.1 DisplayPort Routing Guidelines

Carriers that support DisplayPort (DisplayPort only or dual mode):

- DC blocking capacitors shall be placed on the Carrier for the DP_PAIR[0:3] signals.
- The Carrier shall include a blocking FET on DP_HPD to prevent back-drive current from damaging the Module.

When implementing DisplayPort on the Carrier Board, the DP_AUX+ line shall have a pulldown resistor to GND. The resistor value should be 100kΩ. The DP_AUX- line shall have a pull-up resistor to 1.8V. The resistor value should be 100kΩ. The DP_HPD signal shall include a blocking FET to prevent back-drive current damage. The DP_HPD signal shall be pulled-down to GND with a 110kΩ resistor.

The DP signals can be used to support a variety of video interfaces. The circuits required to realize the different video interfaces will be determined by a future SMACR Carrier Design Guide subcommittee. At this time, they only requirement placed on Modules for the DP signals is the maximum trace length specified.

Figure 27: Topology for DisplayPort

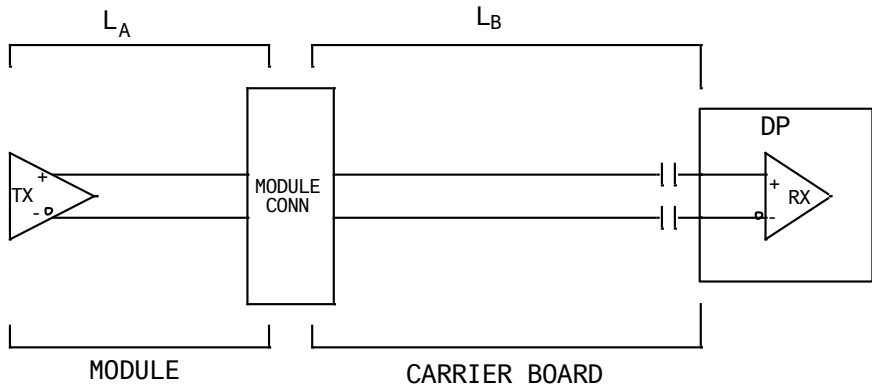


Table 38: DisplayPort Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	DisplayPort	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pair	Min. 20mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mil	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to DP connector: 7” AUX channel: 17”	
Length matching	Differential pairs (intra-pair): Max. ±2.5 mils For each channel, match the lengths of the differential pairs (Inter-Pair) to be within a 250 mil window (max length – min length < 250mil).	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	

Notes:

2.12.3.2 HDMI Routing Guidelines

High-Definition Multimedia Interface (HDMI) is a licenseable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TMDS video stream.

The SMARC specification defines a single-link HDMI interface with a pixel clock rate of up to 165 MHz. This interface is shared with the DisplayPort signals.

Figure 28: Topology for HDMI

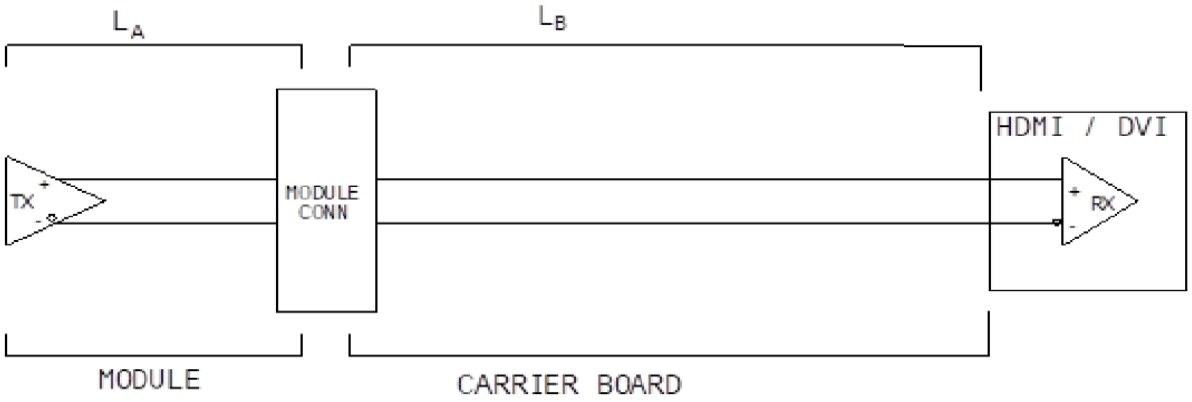


Table 39: HDMI Connector / Device Down Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	HDMI	
Differential Impedance Target	85 Ω ±10%	
Single End	50Ω ±10%	
Spacing between pairs-to-pair	Min. 15mil	
Spacing between differential pairs and high-speed periodic signals	Min. 15mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 15mil	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	DDI differential pairs to Active Level Shifter: 9” DDC channel: 17”	
Length matching	Differential pair length mismatch: Max. ±2.5 mils Inter-pair length mismatch For HDMI*1.4 signals is ± 0.9” For HDMI*2.0 signals is ± 0.5”	
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	
Carrier Board Via Usage	Max. 2 vias.	
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	

Notes:

2.12.4 ESD Protection

HDMI signals are subjected to ESD strikes due to plugging in of the devices through the HDMI cable and frequent human contact that can destroy both the HDMI host and devices on the platform. Therefore these ports need to be protected.

There are a wide variety of ESD protection devices and ESD suppressors readily available in the market such as Metal Oxide Varistors (MOVs), Zener Diode, Transient Voltage Suppressor (TVS), Polymer devices and ESD diode arrays. With 1.65 Gbps of data rate, HDMI is very sensitive to parasitic capacitance. Excessive parasitic capacitance can severely degrade the signal integrity and lead to a compliance or operational failure. To maintain signal integrity, Intel recommends to use ESD suppressors or diode arrays having a low junction capacitance.

Recommended characteristics of an ideal ESD Protection Diode for HDMI:

- Able to withstand at least 8 kV of ESD strikes.
- Low capacitance <1 pF to minimize signal distortion at high data rates as higher capacitance degrade the HDMI signal quality.
- Fast response/rise time to protect from the fast rise time of ESD surge pulses.
- Low-leakage current to minimize static power consumption.
- Ensure the selected ESD solution will not violate HDMI Voff spec. In a low power state a power rail ESD diode can become forward biased as a result on the HDMI sink (panel) termination of 50 Ω to 3.3 V
- Some ESD devices may impact the trace impedance. Care should be taken while choosing such devices so that the differential-impedance target in the *HDMI 1.4 Specification* is not violated.

The *HDMI 1.4a Specification* requires that 8 kV of ESD strikes be tolerated.

The ESD protection devices should be placed as close to the HDMI connector as possible so that when ESD strikes occur, the discharges can be quickly absorbed or diverted to the ground/power plane before it is coupled to another signal path nearby.
Footprints for ESD components or diode arrays can be provided on board with no stubs and no more than 750 mils (19.05 mm) from the connector. The ESD components can be stuffed depending on the requirement.

2.13 Camera Interfaces(MIPI CSI) SOM-2532 is no support CSI.

SMARC 2.0 defines two MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1 *may* be implemented with up to four differential data lanes (CSI1_D[0:3]+/- signals) to support higher resolution cameras.
Both MIPI CSI interfaces support MIPI-CSI 2.0 but are also prepared to support the implementation of MIPI-CSI 3.0. Both standards continue to evolve (see http://mipi.org/specifications/camera-interface).
While MIPI-CSI 2.0 utilizes an I2C bus (I2C_CAM[0:1]) to communicate with the camera the MIPI-CSI 3.0 uses a differential data lane (CSI[0:1]_TX+/-).

Camera I2C Support:

The I2C_CAM_ port is intended to support serial cameras. Most contemporary cameras with I2C support allow a choice of two I2C address ranges.

MIPI CSI Configuration CSI-2 and CSI-3:

The newer version of the MIPI Camera Serial Interface CSI-3 no longer uses an I2C bus to transmit commands configurations to the camera. A newly defined high speed differential signal pair is used instead.

Serial Cameras In:

Two MIPI CSI camera interfaces are supported. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes. MIPI CSI 2.0 and MIPI CSI 3.0 are supported. With SMARC 2.11 the fill order changed to CSI1 first.

Camera Data Interface Formats:

There are a wide variety of data formats that are used to convey camera data to a host system. A complete description of these formats is very much beyond the scope of this design guide. Briefly stated, camera data formats may be divided into two groups: “raw” and “processed”. The raw camera data formats need to be adjusted for camera and sensor specific characteristics (non-linearities, sensor pixel quirks, color corrections and so on). Using the raw format requires an additional level of software complexity that is beyond many users. Unless you have a specific need for a particular camera that outputs “raw” sensor data, it is best to stick with cameras that include a processor on the camera module that convert the camera sensor data to a standard format such as RGB or YUV, JPEG or others. The “Bayer” format is one of the numerous raw formats that you may wish to avoid. A variation on the above is that some cameras offer “raw” RGB, meaning that the pixel data is sorted into RGB elements but sensor nonlinearities are not processed in the camera IC.

2.13.1 Camera Configurations

Configuration	CSI0	CSI1
Serial	CSI0 - 2 lanes MIPI CSI 2.0	CSI1 – 2 or 4 lanes MIPI-CSI 2.0
Altemative	CSI0 - 2 lanes MIPI CSI 3.0	CSI1 – 2 or 4 lanes MIPI-CSI 3.0

2.13.2 Camera Signal Definition

Table 40: Camera Interface Signal Definition

Signal	Pin#	Description	I/O	Note
GPIO0 / CAM0_PWR#	P108	Camera 0 Power Enable, active low output. Carrier Board: Device - Connect to Camera0 device pin PWR0. Camera Connector - Connect to Camera0 Conn pin PWR0 Enable. N/C if not used.	O COMS Runtime 1.8V	4
GPIO1 / CAM1_PWR#	P109	Camera 1 Power Enable, active low output. Carrier Board: Device - Connect to Camera1 device pin PWR1. Camera Connector - Connect to Camera1 Conn pin PWR1 Enable. N/C if not used.	O COMS Runtime 1.8V	4
GPIO2 / CAM0_RST#	P110	Camera 0 Reset, active low output. Carrier Board: Device - Connect to Camera0 device pin RST0. Camera Connector - Connect to Camera0 Conn pin RST 0 Enable. N/C if not used.	O COMS Runtime 1.8V	4
GPIO1 / CAM1_RST#	P111	Camera 1 Reset, active low output. Carrier Board: Device - Connect to Camera1 device pin RST1. Camera Connector - Connect to Camera1 Conn pin RST1 Enable. N/C if not used.	O COMS Runtime 1.8V	4

Signal	Pin#	Description	I/O	Note
CSI0_TX- / I2C_CAM0_DAT	S7	I2C data: Serial camera support link for serial cameras Alternative function: CSI0_TX- for MIPI CSI 3.0 CSI0_TX-: Differential data pairs used for camera configurations. This signal has 1K Ω pull up to 1.8V on the module. Carrier Board: Device - Connect to Camera0 device pin DAT0. Camera Connector - Connect to Camera0 Conn pin DAT0. N/C if not used.	DAT: I/O OD CMOS TX-: O M-PHY Runtime 1.8V	1,3
CSI0_TX+ / I2C_CAM0_CK	S5	I2C clock: Serial camera support link for serial cameras Alternative function: CSI0_TX+ for MIPI CSI 3.0 CSI0_TX+: Differential data pairs used for camera configurations. This signal has 1K Ω pull up to 1.8V on the module. Carrier Board: Device - Connect to Camera0 device pin CK0. Camera Connector - Connect to Camera0 Conn pin CK0. N/C if not used.	CK: I/O OD CMOS TX+: O M-PHY Runtime 1.8V	2,3
CSI1_TX+ / I2C_CAM1_CK	S1	I2C clock: Serial camera support link for serial cameras Alternative function: CSI1_TX+ for MIPI CSI 3.0 CSI1_TX+: Differential data pairs used for camera configurations. This signal has 1K Ω pull up to 1.8V on the module Carrier Board: Device - Connect to Camera1 device pin CK1. Camera Connector - Connect to Camera1 Conn pin CK1. N/C if not used.	CK: I/O OD CMOS TX+: O M-PHY Runtime 1.8V	2,3
CSI1_TX- / I2C_CAM1_DAT	S2	I2C data: Serial camera support link for serial cameras Alternative function: CSI1_TX- for MIPI CSI 3.0 CSI1_TX-: Differential data pairs used for camera configurations. This signal has 1K Ω pull up to 1.8V on the module. Carrier Board: Device - Connect to Camera1 device pin DAT1. Camera Connector - Connect to Camera1 Conn pin DAT1. N/C if not used.	DAT: I/O OD CMOS TX-: O M-PHY Runtime 1.8V	1,3

Signal	Pin#	Description	I/O	Note
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock inputs. Carrier Board: Device – CSI0_CK+ Connect to Camera0 device pin CSI0_CK+. CSI0_CK- Connect to Camera0 device pin CSI0_CK-. Camera Connector – CSI0_CK+ Connect to Camera0 Conn pin CSI0_CK+. CSI0_CK- Connect to Camera0 Conn pin CSI0_CK-. N/C if not used.	I D-PHY Runtime	3
CSI0_RX0+ CSI0_RX0-	S11 S12	CSI0 differential data inputs. Carrier Board: Device – CSI0_RX0+ Connect to Camera0 device pin CSI0_D0+. CSI0_RX0- Connect to Camera0 device pin CSI0_D0-. Camera Connector – CSI0_RX0+ Connect to Camera0 Conn pin CSI0_D0+. CSI0_RX0- Connect to Camera0 Conn pin CSI0_D0-. N/C if not used.	I D-PHY / I M-PHY Runtime	3
CSI0_RX1+ CSI0_RX1-	S14 S15	CSI0 differential data inputs. Carrier Board: Device – CSI0_RX1+ Connect to Camera0 device pin CSI0_D1+. CSI0_RX1- Connect to Camera0 device pin CSI0_D1-. Camera Connector – CSI0_RX1+ Connect to Camera0 Conn pin CSI0_D1+. CSI0_RX1- Connect to Camera0 Conn pin CSI0_D1-. N/C if not used.	I D-PHY / I M-PHY Runtime	3
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock inputs. Carrier Board: Device – CSI1_CK+ Connect to Camera1 device pin CSI1_CK+. CSI1_CK- Connect to Camera1 device pin CSI1_CK-. Camera Connector – CSI1_CK+ Connect to Camera1 Conn pin CSI1_CK+. CSI1_CK- Connect to Camera1 Conn pin CSI1_CK-. N/C if not used.	I D-PHY Runtime	3

Signal	Pin#	Description	I/O	Note
CSI1_RX0+ CSI1_RX0-	P7 P8	CSI1 differential data inputs. Carrier Board: Device – CSI1_RX0+ Connect to Camera1 device pin CSI1_D0+. CSI1_RX0- Connect to Camera1 device pin CSI1_D0-. Camera Connector – CSI1_RX0+ Connect to Camera1 Conn pin CSI1_D0+. CSI1_RX0- Connect to Camera1 Conn pin CSI1_D0-. N/C if not used.	I D-PHY / I M-PHY Runtime	3
CSI1_RX1+ CSI1_RX1-	P10 P11	CSI1 differential data inputs. Carrier Board: Device – CSI1_RX1+ Connect to Camera1 device pin CSI1_D1+. CSI1_RX1- Connect to Camera1 device pin CSI1_D1-. Camera Connector – CSI1_RX1+ Connect to Camera1 Conn pin CSI1_D1+. CSI1_RX1- Connect to Camera1 Conn pin CSI1_D1-. N/C if not used.	I D-PHY / I M-PHY Runtime	3
CSI1_RX2+ CSI1_RX2-	P13 P14	CSI1 differential data inputs. Carrier Board: Device – CSI1_RX2+ Connect to Camera1 device pin CSI1_D2+. CS1I_RX2- Connect to Camera1 device pin CSI1_D2-. Camera Connector – CSI1_RX2+ Connect to Camera1 Conn pin CSI1_D2+. CSI1_RX2- Connect to Camera1 Conn pin CSI1_D2-. N/C if not used.	I D-PHY / I M-PHY Runtime	3
CSI1_RX3+ CSI1_RX3-	P16 P17	CSI1 differential data inputs. Carrier Board: Device – CSI1_RX3+ Connect to Camera1 device pin CSI1_D3+. CSI1_RX3- Connect to Camera1 device pin CSI1_D3-. Camera Connector – CSI1_RX3+ Connect to Camera1 Conn pin CSI1_D3+. CSI1_RX3- Connect to Camera1 Conn pin CSI1_D3-. N/C if not used.	I D-PHY / I M-PHY Runtime	3

Signal	Pin#	Description	I/O	Note
CAM_MCK	S6	Master clock output for CSI camera support (may be used for CSI0 and / or CSI1) Carrier Board: Device – CAM_MCK Connect to Camera device pin XVCLK. Camera Connector – CAM_MCK Connect to Camera Conn pin XVCLK. N/C if not used.	O CMOS Runtime 1.8V	3

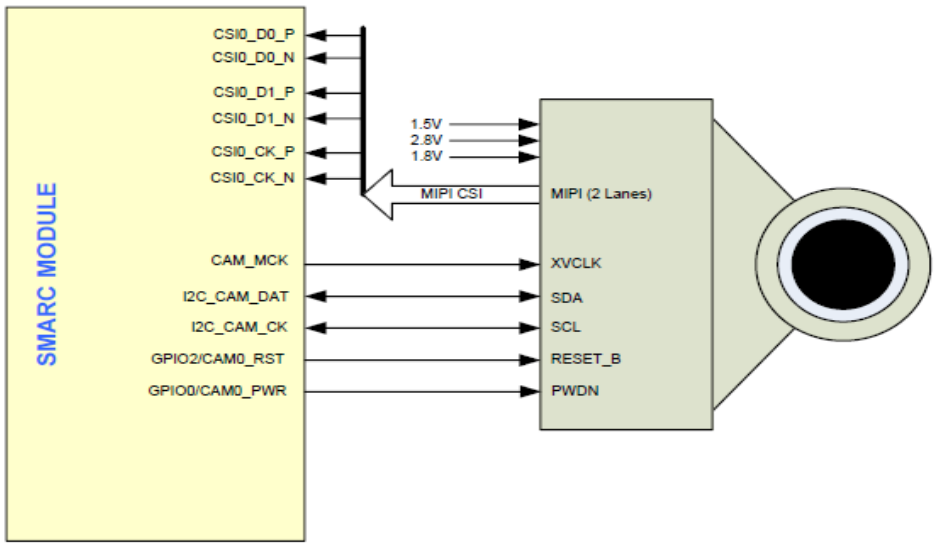
Note:

1. MIPI-CSI 2.0 uses I2C_CAM0_DAT which requires PU MIPI-CSI 3.0 uses CSI0_TX-, no PU required
2. MIPI-CSI 2.0 uses I2C_CAM0_CK which requires PU MIPI-CSI 3.0 uses CSI0_TX+, no PU required
3. SOM-2532 is no support CIS. It's NC pin.
4. GPIO only.

2.13.3 Serial Camera Interface Example

The figure below illustrates a CSI implementation on a SMARC Carrier. Here, the output of the sensor is connected to CSI0 interface of the SMARC Module. I2C_CAM is the control interface used for configuring the sensor. CAM_MCK is the master clock output from the SMARC Module.

Figure 29: Serial Camera Implementation



2.13.4 Other Camera Options

SMARC systems have the option of using the dedicated SMARC camera interface pin set. For a dedicated system produced in high volume, this is likely to be the most cost effective option. However, other options exist. USB cameras are becoming very popular. They enjoy good software support and are becoming more and more cost effective as time passes. However, the bandwidth of a HS USB interface (480 Mbps) is less than what is possible with the SMARC CSI camera interfaces.

2.13.5 Camera (MIPI CSI) Routing Guidelines

NA

2.13.6 Camera (MIPI CSI) Trace Length Guidelines

Figure 30: Topology for MIPI CSI

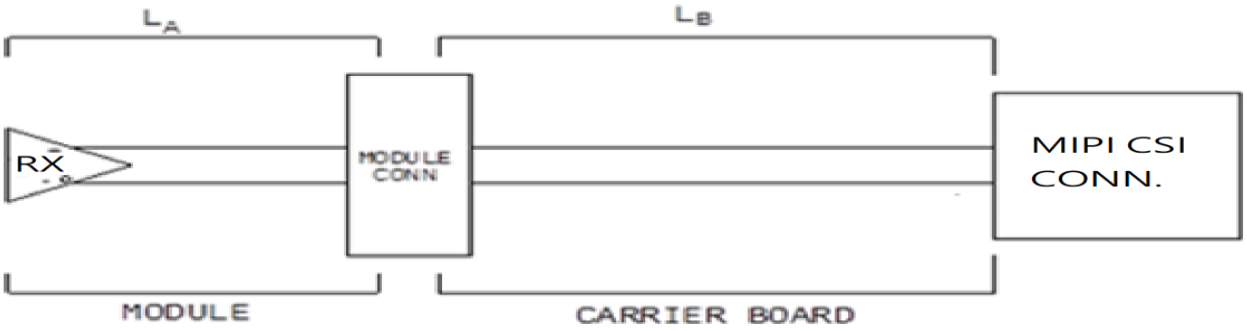


Table 41: MIPI CSI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	CSI	1
Differential Impedance Target	85 Ω ±10%	1
Single End	50Ω ±10%	1
Isolation to equivalent pairs	15 mils (MS) and 15 mils (DS)	1
Isolation to other signal groups	15 mils (MS) and 15 mils (DS)	1
LA	NA	1
LB	Carrier Board Length	1
Max length of LA+LB	CSI differential pairs to CSI connector: X”	1
Length matching	Length Matching between P and N within a diff. pair: Max. ±X mils Length Matching between Data and Clock: . Max. ±X mils	1
Reference Plane	GND referencing preferred. Min 40-mil trace edge-to-major plane edge spacing.	1
Carrier Board Via Usage	Max. 3 vias.	1

Notes:

1. SOM-2532 is no support CIS.

2.13.7 Camera (MIPI CSI) – Connector and Cable

Table 42: MIPI CSI Connector and Cable Requirement

Parameter	Specification	Description/Comments
Connector differential Impedance	90 Ω	
Connector differential Insertion Loss	1. ≥ -0.026 db @ 20MHz 2. ≥ -0.035 db @ 0.5 Ghz 3. ≥ -0.046 db @ 0.75 Ghz 4. ≥ -0.109 db @ 1.5 Ghz 5. ≥ -0.195 db @ 2.15 Ghz	Frequency domain measurement, Text fixture deembedded
Connector differential Return Loss	1. ≤ -57.14 db @ 20 MHz 2. ≤ -27.1 db @ 0.5 Ghz 3. ≤ -23.23 db @ 0.75 Ghz 4. ≤ -17.64 db @ 1.5 Ghz 5. ≤ -14.62 db @ 2.15 Ghz	
Connector differential Near End Crosstalk	1. ≤ -79.16 db @ 20 MHz 2. ≤ -68.16 db @ 0.5 Ghz 3. ≤ -64.84 db @ 0.75 Ghz 4. ≤ -59.01 db @ 1.5 Ghz 5. ≤ -55.96 db @ 2.125 Ghz	
Cable differential impedance	90Ω±10%	
Cable differential Insertion Loss per inch	1. ≥ -0.044 db @ 20MHz 2. ≥ -0.165 db @ 0.5 GHz 3. ≥ -0.223 db @ 0.75 GHz 4. ≥ -0.37 db @ 1.5 GHz 5. ≥ -0.45 db @ 2.15 GHz	Frequency domain measurement, Text fixture deembedded
Cable differential Return Loss per inch	1. ≤ -46.1 db @ 20 MHz 2. ≤ -26.1 db @ 0.5 GHz 3. ≤ -23.23 db @ 0.75 GHz 4. ≤ -19.6 db @ 1.5 GHz 5. ≤ -20.34 db @ 2.15 GHz	
Cable differential Near End Crosstalk per inch	1. ≤ -76.89 db @ 20 MHz 2. ≤ -48.57 db @ 0.5 GHz 3. ≤ -45.6 db @ 0.75 GHz 4. ≤ -42.22 db @ 1.5 GHz 5. ≤ -43.07 db @ 2.125 GHz	
Cable Intra pair skew	≤ 5 ps	Time delay difference between p and n of a differential pair

2.14 CAN Interface

General:

The CAN (“Controller Area Network”) bus is a differential half duplex data bus used in automotive and industrial settings. A CAN bus uses shielded or unshielded twisted differential pair wiring, terminated in the pair differential impedance of 120 ohms at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion, although stubs of up to 0.3 meters are allowed at each node. The standard allows data rates of up to 1 Mbps, with a maximum bus length of 40 meters at that rate. Various slower rates are defined, along with longer and longer bus lengths allowed as the data rates go down. A bus rate of 250 kbps is in common use in automotive situations. With CAN FD also faster baud rates are possible. The two lines in a CAN twisted pair are referred to as CAN_H and CAN_L (for CAN High and CAN Low). There are two bus states on the CAN physical layer: the Dominant state and the Recessive state. In the Dominant state, CAN_L is pulled to GND through an open drain driver and CAN_H is pulled to the CAN Vcc through an open drain driver. In the Recessive state, CAN_L and CAN_H are not actively driven and they are pulled to a voltage of (Vcc / 2) by passive components. Hence the CAN bus is essentially a differential open-drain bus. On the system logic side of a CAN transceiver, the CAN Dominant state is a logic low and the Recessive state a logic high.

The CAN protocol has features important to a real time environment:

Nodes are prioritized: CAN nodes are assigned an 11 bit identifier

o The lower the ID number, the higher priority

Latency time is guaranteed

Data packets are limited to 8 bytes maximum

o Higher level protocols take care of handling large data sets

The bus has Multi-master capability

There are error detection and signaling features

The CAN bus base standard is defined by ISO 11898-1:2003, available for a fee from the ISO (www.iso.org). There are some very helpful CAN application notes from Texas Instruments (a vendor of CAN MAC and transceiver devices) available for free. These include “*Introduction to the Controller Area Network (CAN)*”, TI document number SLOA101A, and “*Controller Area Network Physical Layer Requirements*”, document number SLLA270. The original CAN bus protocol definition by Bosch is also freely available on the web (*CAN Specification*, Version 2.0 © 1991 Robert Bosch GmbH).

Various connectors are used in CAN bus implementations. The use of DB-9 connectors is fairly common. The TI application note (SLLA270) referenced above has pin-out information for a couple of common CAN connector implementations.

SMARC Implementation:

The SMARC specification allows for up to two logic level CAN ports. The ports run at the Module I/O voltage (typically 1.8V) and consist of an asynchronous CAN TX line and an RX line from and to the SMARC Module CAN protocol controller.

A Carrier based CAN transceiver is required to create a SMARC system CAN implementation. CAN PHYs are available from Texas Instruments, On Semiconductor, NXP, Freescale, Microchip and numerous other vendors. The logic interface for CAN PHYs is typically suited for 3.3V logic I/O, so level translation is required if the SMARC Module is running 1.8V I/O.

Precautions must be taken to prevent a CAN system from sending out frames or blocking a CAN-Bus unintentionally, for example during reset and power down. During power down, CAN Transceivers are designed to be HIGH-Z. During power up or reset, they must be put into a “listen only mode”. It is the responsibility of the application software to activate the CAN-transceiver after all initialization is done.

2.14.1 CAN interface Signal Definitions

Table 43: CAN interface Signal Definitions

Signal	Pin#	Description	I/O	Note
CAN0_TX	P143	Transmit Line for CAN Carrier Board: Connect to CAN Bus transceiver transmit data input TXD pin N/C if not used	O CMOS Runtime 1.8V	
CAN0_RX	P144	Receive Line for CAN Carrier Board: Connect to CAN Bus transceiver receive data output RXD pin N/C if not used	I CMOS Runtime 1.8V	
CAN1_TX	P145	Transmit Line for CAN Carrier Board: Connect to CAN Bus transceiver transmit data input TXD pin N/C if not used	O CMOS Runtime 1.8V	
CAN1_RX	P146	Receive Line for CAN Carrier Board: Connect to CAN Bus transceiver receive data output RXD pin N/C if not used	I CMOS Runtime 1.8V	

Note:

2.14.2 CAN interface Routing Guidelines

It should be routed as a differential pair signal with 120 Ohm differential impedance. The end points of CAN bus should be terminated with 120 Ohms or with 60 Ohms from the CAN_H line and 60 Ohms from the CAN_L line to the CAN Bus reference voltage. Check your CAN transceiver application notes for further details on termination.

2.14.3 CAN interface Trace Length Guidelines

Figure 31: Topology for CAN interface

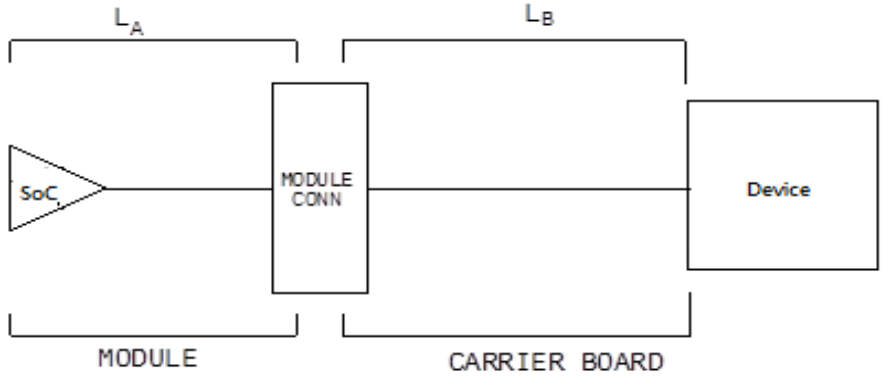


Table 44: CAN interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	CAN interface	
Single End	NA	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	ASAP	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.15 SPI – Serial Peripheral Interface Bus

The SPI (Serial Peripheral Interface) is a full duplex synchronous bus supporting a single master and multiple slave devices. The SPI bus consists of a serial clock line (generated by the master); data output line from the master; a data input line to the master and one or more active low chip select signals (output from the master).

Clock frequencies from 1-100MHz may be generated by the master depending on the maximum frequency supported by the components in the system. SMARC Modules running a 1.8V I/O interface are generally limited to about a 50 MHz clock rate on this interface.

The SMARC Module will always be the SPI master. SMARC Modules may support a Carrier SPI Boot option.

Each SPI device requires a chip select, a clock, a data in line and a data out line. The device I/O level must of course be compatible with the SMARC Module I/O level.

The Carrier SPI0 device may be selected as the Boot Device.

SPI1 is the general-purpose SPI bus.

2.15.1 SPI0 Signal Definition

Table 45: SPI0 Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SPI0_CS0#	P43	SPI0 chip select 0 output. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	
SPI0_CS1#	P31	SPI0 Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	
SPI0_DIN	P45	Data in to Module from Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data Out pin 2 Device - Serial Data Out pin N/C if not used	I CMOS Standby 1.8V	

Signal	Pin#	Description	I/O	Note
SPI0_DO	P46	Data out from Module to Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data In pin 5 Device - Serial Data In pin N/C if not used	O CMOS Standby 1.8V	
SPI0_CLK	P44	Clock from Module to Carrier SPI Connect to SPI Flash - Series Clock pin 6 Device - Series Clock N/C if not used	O CMOS Standby 1.8V	

Note:

2.15.2 SPI1 Signal Definition *SOM-2532 is not supported SPI1.

Table 46: SPI1 Interface Signal Definition

Signal	Pin#	Description	I/O	Note
SPI1_CS0#	P54	SPI1 chip select 0 output. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	1
SPI1_CS1#	P55	SPI1 Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used. Carrier Board: Connect to SPI Flash - Chip Select pin 1 Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	1
SPI1_DIN	P57	Data in to Module from Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data Out pin 2 Device - Serial Data Out pin N/C if not used	I CMOS Standby 1.8V	1
SPI1_DO	P58	Data out from Module to Carrier SPI Carrier Board: Connect to SPI Flash - Serial Data In pin 5 Device - Serial Data In pin N/C if not used	O CMOS Standby 1.8V	1
SPI1_CLK	P56	Clock from Module to Carrier SPI Connect to SPI Flash - Series Clock pin 6 Device - Series Clock N/C if not used	O CMOS Standby 1.8V	1

Note:

1. SOM-2532 is not supported SPI1.

2.15.3 QSPI Signal Definition *SOM-2532 is not supported QSPI.

The QSPI is a controller extension for the SPI Bus. The difference is that it uses a data queue with programmable queue pointers that allow the data transfers without the CPU intervention. It also has a wrap-around mode that allows continuous transfers and from the queue with no CPU intervention. The peripherals appear to the CPU as memory-mapped parallel devices. This is useful in application such as controlling an analog to digital converter. QSPI has some more programmable features like chip select and transfer length delay.

Table 47: QSPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
QSPI_CS0#	P54	QSPI Master chip select 0 output. Carrier Board: Connect to SPI Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	1
QSPI_CS1#	P55	QSPI Master chip select 1 output. Carrier Board: Connect to SPI Device - Chip Select pin N/C if not used	O CMOS Standby 1.8V	1
QSPI_IO_3	S57	QSPI Data input / output Carrier Board: Connect to SPI Device - Serial Data Out pin N/C if not used	I/O CMOS Standby 1.8V	1
QSPI_IO_2	S56	QSPI Data input / output Carrier Board: Connect to SPI Device - Serial Data Out pin N/C if not used	I/O CMOS Standby 1.8V	1
QSPI_IO_1	P57	QSPI Data input / output Carrier Board: Connect to SPI Device - Serial Data Out pin N/C if not used	I/O CMOS Standby 1.8V	1
QSPI_IO_0	P58	QSPI Data input / output Carrier Board: Connect to SPI Device - Serial Data Out pin N/C if not used	I/O CMOS Standby 1.8V	1
QSPI_CLK	P56	Clock from Module to Carrier SPI Carrier Board: Connect to SPI Device - Series Clock N/C if not used	O CMOS Standby 1.8V	1

Note:

1. SOM-2532 is not supported QSPI.

2.15.4 SPI Routing Guidelines

NA

2.15.5 SPI Trace Length Guidelines

Figure 32: Topology for SPI

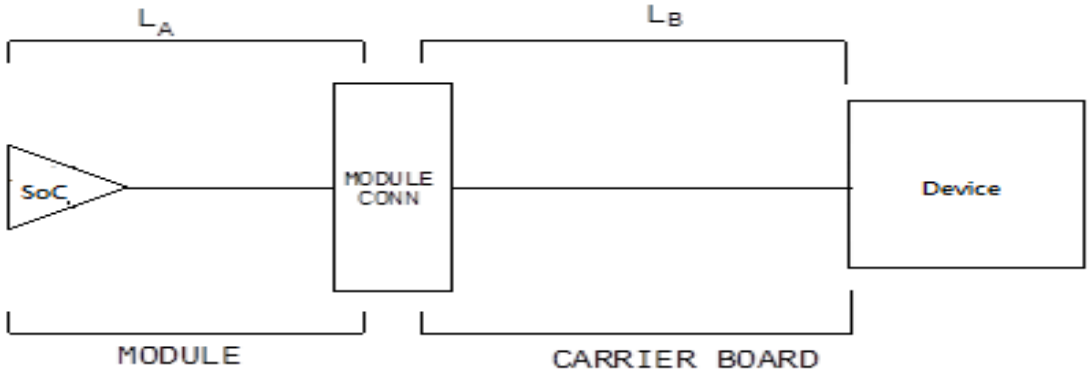


Table 48: SPI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	SPI	1
Single End	50Ω ±15%	1
Nominal Trace Space within SPI Signal Group	Min. 10mils	1
Spacing to Other Signal Group	Min. 15mils	1
LA	Please see the SOM-2532 Layout Checklist	1
LB	Carrier Board Length	1
Max length of LA+LB	7”	1
DATA to CLK Maximum Pin to Pin Length Mismatch	Max. 500mils	1
Via Usage	Try to minimize number of vias	1

Notes:

1. SOM-2532 is not supported SPI1 and QSPI.

2.16 eSPI Interface

The Enhanced Serial Peripheral Interface (eSPI) provides an alternative for connecting an EC to the platform.

eSPI operates at 1.8V only and supports one slave device. This interface is not shared and distinct from the SPI interface used for flash device and TPM. The eSPI interface supports 20 MHz, 24MHz, 30 MHz, 48 MHz, and 60 MHz and up to Quad Mode.

2.16.1 eSPI Signal Definition

Table 49: eSPI Interface Signal Definition

Signal	Pin#	Description	I/O	Note
ESPI_CS0#	P54	ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. Carrier Board: Connect to eSPI Device – eSPI_CS0# N/C if not used	O CMOS Standby 1.8V	
ESPI_CS1#	P55	ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select# A low selects a particular eSPI slave for the transaction. Each of the eSPI slaves is connected to a dedicated Chip Selectn# pin. Carrier Board: Connect to eSPI Device – eSPI_CS1# N/C if not used	O CMOS Standby 1.8V	
ESPI_IO_0 ESPI_IO_1 ESPI_IO_2 ESPI_IO_3	P58 P57 S56 S57	ESPI Master Data Input / Outputs These are bi-directional input/output pins used to transfer data between master and slaves. In Single I/O mode, ESPI_IO_0 is the eSPI master output/eSPI slave input (MOSI) whereas ESPI_IO_1 is the eSPI master input/eSPI slave output (MISO). Carrier Board: Connect to eSPI Device – eSPI_IO0, eSPI_IO1, eSPI_IO2, eSPI_IO3, the Carrier ***shall*** have a 33 Ω series termination. N/C if not used	I/O CMOS Standby 1.8V	

Signal	Pin#	Description	I/O	Note
ESPI_ALERT0# ESPI_ALERT1#	S43 S44	This pin is used by eSPI slave to request service from eSPI master. Alert# is an open-drain output from the slave. This pin is optional for Single Master-Single Slave configuration where I/O[1] can be used to signal the Alert event. Carrier Board: Connect to eSPI Device – eSPI_ALERT0#, eSPI_ALERT1#. N/C if not used.	I OD CMOS Standby 1.8V	
ESPI_RESET#	S58	eSPI Reset Reset the eSPI interface for both master and slaves. eSPI Reset# is typically driven from eSPI master to eSPI slaves. Carrier Board: Connect to eSPI Device – eSPI_RESET# N/C if not used	O CMOS Standby 1.8V	
ESPI_CK	P56	eSPI Master Clock Output This pin provides the reference timing for all the serial input and output operations. Carrier Board: Connect to eSPI Device – eSPI_CLK, the Carrier ***shall*** have a 33 Ω series termination. N/C if not used	O CMOS Standby 1.8V	

Note:

2.16.2 eSPI/SPI1/QSPI Pin Sharing

Pin #	eSPI Name	SPI1 Name	QSPI Name
P58	ESPI_IO_0	SPI1_DO	QSPI_IO_0
P57	ESPI_IO_1	SPI1_DIN	QSPI_IO_1
S56	ESPI_IO_2	-	QSPI_IO_2
S57	ESPI_IO_3	-	QSPI_IO_3
S43	ESPI_ALERT0#	-	-
S44	ESPI_ALERT1#	-	-
S58	ESPI_RESET	-	-
P56	ESPI_CK	SPI1_CK	QSPI_CK
P55	ESPI_CS1#	SPI1_CS1#	QSPI_CS1#
P54	ESPI_CS0#	SPI1_CS0#	SPI_CS0#

2.16.3 eSPI Routing Guidelines

2.16.3.1 eSPI Devices

At the time of this writing, the use case and design rules for eSPI are still being developed.

Designers of Modules and Carriers are provided with the following guidance:

The maximum trace length for Carrier routed eSPI traces ***shall not*** exceed 4.5”.

Carrier routed eSPI traces ***shall*** be routed at 50 Ohms.

Carrier routed eSPI traces ***shall*** have 5 mil via to via clearance, 4 mil trace to via clearance, and 10 mil clearance to any other traces.

The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_CK signal.

The Carrier ***shall*** have a 33 Ohm series termination between 0.5” and 1” of the target device on the ESPI_IO_[0..3] signals.

The Carrier ***shall*** length match ESPI_CK and ESPI_IO_[0..3] within 250mils.

The Carrier ***shall*** length match ESPI_CK and ESPI_CS within 100mils.

2.16.4 eSPI Trace Length Guidelines

Figure 33: Topology for eSPI

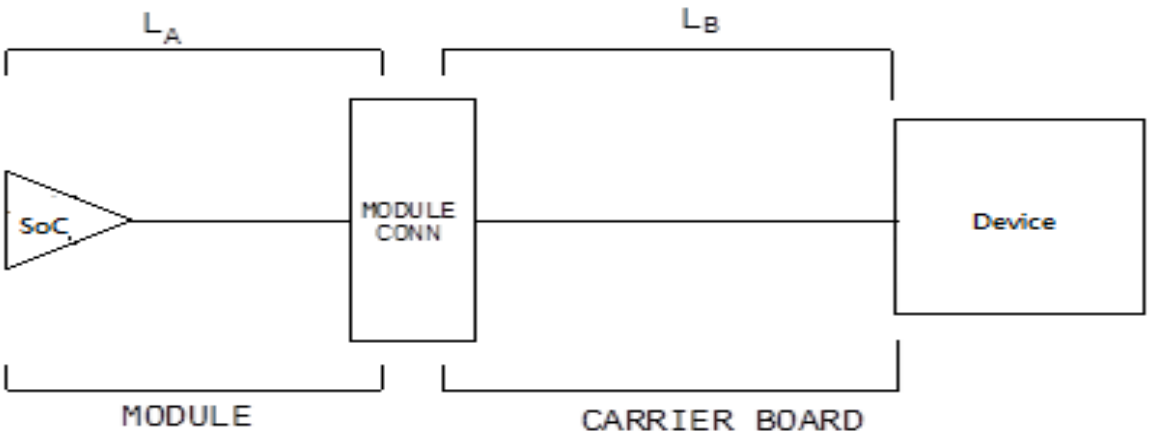


Table 50: eSPI Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	eSPI	
Single End	50Ω ±15%	
Nominal Trace Space within eSPI Signal Group	Trace spacing between DATA and DATA is 5 mils (0.127mm) Trace spacing between CLK and other signals is 15 mils (0.381mm)	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	6”	
Length matching between data signals	eSPI clock and eSPI data must be length matched to within 500 mils (12.7mm).	
Length matching between CS# signals	eSPI clock and eSPI CS# must be length matched to within 1000 mils (25.4mm).	
Reference Plane	GND referencing preferred.	
Via Usage	Try to minimize number of vias	

Notes:

2.17 I2C Interface

The Module supports six I2C interfaces, per the following table. Except for the LCD and HDMI Module I2C interfaces, the I2C ports ***should*** be multi-master capable. Data rates of 100 kHz and 400 kHz ***should*** be supported.

The I2C bus is a versatile low bandwidth multi-drop bus originally defined by Philips (now NXP). It is a two wire bus (clock and data) that relies on the use of open-drain drivers and passive pull-ups. The bus can be single master or multi-master. SMARC Modules are always I2C masters. Whether or not they allow other masters is Module implementation dependent. Most SMARC systems use the I2C bus as a way for the SMARC I2C Masters to interface to a variety of I2C Slave peripherals. The standard I2C interface operation speeds are 100 kHz and 400 kHz. Some implementations allow faster speeds.

All I2C interfaces but the I2C_GP interface are described in the section served by that I2C link (LCD, HDMI, Camera Interface, etc).

Table 51: Six I2C interfaces

I2C Port	Primary Purpose	Alternate Use	I/O Voltage Level
I2C_PM	Power Management support	System configuration management	I/O CMOS Standby/Sleep 1.8V
I2C_CAM0 I2C_CAM1 I2C_CAM2 I2C_CAM3	Camera support	General Purpose	I/O OD CMOS Runtime 1.8V
I2C_GP	General purpose use		I/O OD CMOS Runtime 1.8V
I2C_LCD	LCD display support	General Purpose	I/O OD CMOS Runtime 1.8V
HDMI_CTRL	HDMI control		I/O OD CMOS Runtime 1.8V

2.17.1 I2C Signal Definitions

The I2C_GP Module interface consists of the following two pins.

Table 52: General Purpose I2C Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
I2C_GP_CK	S48	General Purpose I2C Clock output. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to SDA of I2C device N/C if not used	I/O OD CMOS Runtime 1.8V	1
I2C_GP_DAT	S49	General Purpose I2C data I/O line. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to CLK of I2C device. N/C if not used	I/O OD CMOS Runtime 1.8V	1

Note:

1. Default from EC, Chipset is option function.

The SMARC I2C_PM bus is special in that it is used on the Module for power management functions, and it always runs from a 1.8V rail on the Module. The 1.8V voltage rail requirement on the I2C_PM bus allows it to be powered from a simple, low quiescent current linear or buck switching regulator from V_MOD_IN.

On the Module, since it is used for power management, it is “on” even when the Carrier power may be off (i.e. the CARRIER_PW_ON signal may be low, and Carrier circuits that are not involved in power management are powered off).

If the I2C_PM bus is used on the Carrier for functions that are not power management functions, then it needs to be isolated from the Module by a set of back to back FETs.

The SMARC I2C_PM bus may be used on the Carrier for power management functions, such as interfacing to a battery charger or battery fuel gauge.

The SMARC Module specification recommends - but does not require - that Carriers have a parameter EEPROM on the I2C_PM bus, preferably configured as shown here, in the “Module Power Domain”. This, in principle, allows the Module to query the Carrier I2C_PM EEPROM before asserting the CARRIER_PWR_ON signal that enables the main Carrier board power feed.

Table 53: PM I2C Interface Signal Descriptions

Signal	Pin#	Description	I/O	Note
I2C_PM_CK	P121	PM I2C Clock output. Power management I2C bus data and clock. On x86 systems these serve as SMB clock. This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to SDA of I2C device N/C if not used	I/O CMOS Standby/Sleep 1.8V	1
I2C_PM_DAT	P122	PM I2C data I/O line. Power management I2C bus data and clock. On x86 systems these serve as SMB data . This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to CLK of I2C device. N/C if not used	I/O CMOS Standby/Sleep 1.8V	1
SMB_ALERT	P1	SM Bus Alert# (interrupt) signal This signal has 2.2K Ω pull up to 1.8V on the module. Carrier Board: Connect to SMBALERT# of SMBus device. N/C if not used.	I/O CMOS Standby/Sleep 1.8V	

Note:

1. I2C_PM is from EC.

2.17.2 I2C Routing Guidelines

NA

2.17.3 I2C Trace Length Guidelines

Figure 34: Topology for I2C

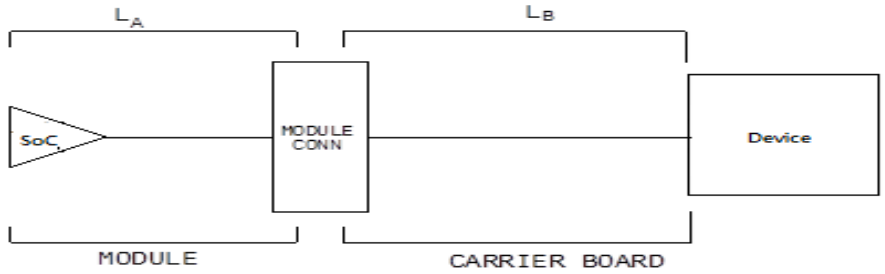


Table 54: I2C Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	I2C	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	Please see the SOM-2532 Layout Checklist	
LB	Carrier Board Length	
Max length of LA+LB	ASAP	
Length Matching between SDA and SCL	Max. 500mils	
Via Usage	Try to minimize number of vias	

Notes:

2.17.4 Connectivity Considerations

The maximum amount of capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by Advantech's Module. The Carrier designer is responsible for ensuring that the maximum amount of capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a general guideline, an IC input has 8pF of capacitance, and a PCB trace has 3.8pF per inch of trace length.

2.18 Asynchronous Serial Ports

Module pins for up to four asynchronous serial ports are defined. The ports are designated SER0 – SER3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only).

RS232 Ports:

The SMARC Module asynchronous serial ports run at 1.8V logic levels. The transmit and receive data lines from and to the Module are active high, and the handshake lines are active low, per industry convention.

If the asynchronous ports are to interface with RS232 level devices, then a Carrier RS-232 transceiver is required. The logic side of the transceiver must be able to run at 1.8V levels. The selection of 1.8V compatible transceivers is a bit limited, although more are appearing with time. Two such devices are the Texas Instruments TRS3253E, and the Maxim MAX13235E. The TI part is more cost effective, but has a top speed of 1 Mbps. The MAX 13235E can operate at maximum speeds over 3 Mbps (but your SMARC Module may or may not - check with Advantech). The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

RS485 Half-Duplex:

This hardware implementation is suitable for multi-drop RS485 networks. The Maxim MAX13451E transceiver accepts 1.8V logic I/O and has other, flexible features of interest such as internal termination options.

Multi-drop RS485 nodes should be strung together in daisy chain fashion using shielded twisted pair cable with a defined differential impedance (usually 120 ohms; sometimes 100 ohm cables are used). The two end-points of the system should be resistively terminated across the pair. The termination value should equal the differential impedance of the twisted pair cable used. The Maxim transceiver allows the termination to be enabled or disabled on the TERM# pin, and can be selected to be 100 ohms or 120 ohms via the TERM100 pin state. These pins can be controlled by Carrier GPIOs if desired.

The RS485 driver is enabled when the SMARC SER2_RTS# signal is asserted low (if the resistor options in front of the XOR gate are loaded as shown, such that the XOR gate inverts the SER2_RTS2# signal for the RS485_DE2 function).

A suitable, likely application specific, software driver is required to make the multi-drop RS485 network work.

2.18.1 Serial interface Signal Definitions

Table 55: Serial interface Signal Definitions

Signal	Pin#	Description	I/O	Note
SER0_TX	P129	Asynchronous serial port data out Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS Runtime 1.8V	1
SER0_RX	P130	Asynchronous serial port data in Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS Runtime 1.8V	1
SER0_RTS#	P131	Request to Send handshake line for SER0 Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 7 RTS# N/C if not used	O CMOS Runtime 1.8V	1
SER0_CTS#	P132	Clear to Send handshake line for SER0 Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 8 CTS# N/C if not used	I CMOS Runtime 1.8V	1
SER1_TX	P134	Asynchronous serial port data out Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS Runtime 1.8V	2
SER1_RX	P135	Asynchronous serial port data in Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS Runtime 1.8V	2

Signal	Pin#	Description	I/O	Note
SER2_TX	P136	Asynchronous serial port data out Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS Runtime 1.8V	1
SER2_RX	P137	Asynchronous serial port data in Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS Runtime 1.8V	1
SER2_RTS#	P138	Request to Send handshake line for SER2 Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 7 RTS# N/C if not used	O CMOS Runtime 1.8V	1
SER2_CTS#	P139	Clear to Send handshake line for SER2 Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 8 CTS# N/C if not used	I CMOS Runtime 1.8V	1
SER3_TX	P140	Asynchronous serial port data out Carrier Board: Device - TXD COM DB-9 port - TxIN of Serial Transceiver and TxOUT to DB-9 pin 3 TXD N/C if not used.	O CMOS Runtime 1.8V	2
SER3_RX	P141	Asynchronous serial port data in Carrier Board: Device - RXD COM DB-9 port - TxOUT of Serial Transceiver and TxIN to DB-9 pin 2 RXD N/C if not used	I CMOS Runtime 1.8V	2

Note:

1. This signal is from chipset.

2. This signal is from EC.

2.18.2 Serial interface Routing Guidelines

NA

2.18.3 Serial interface Trace Length Guidelines

Figure 35: Topology for Serial interface

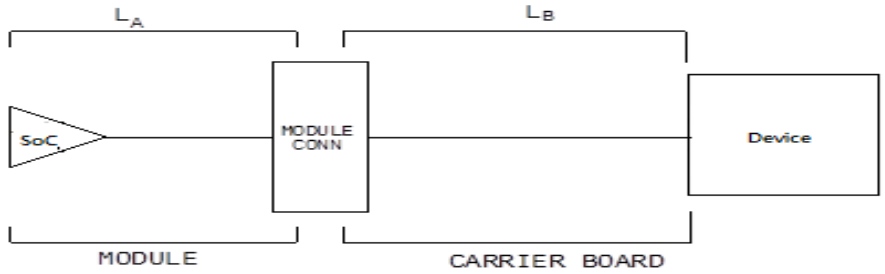


Table 56: Serial interface Trace Length Guidelines

Parameter	Main Route Guidelines	Notes
Signal Group	Serial interface	
Single End	50Ω ±15%	
Nominal Trace Space within SPI Signal Group	Min. 10mils	
Spacing to Other Signal Group	Min. 15mils	
LA	ASAP	
LB	Carrier Board Length	
Max length of LA+LB	NA	
Length Mismatch	NA	
Via Usage	Try to minimize number of vias	

Notes:

2.19 General Purpose Input Output (GPIO)

14 Module pins are allocated for GPIO (general purpose input / output) use. All pins should be capable of bi-directional operation.

At Module power-up, the state of the GPIO pins may not be defined, and may briefly be configured in the "wrong" state, before boot loader code corrects them. Carrier designers should be aware of this and plan accordingly.

All GPIO pins should be weakly pulled up to 1.8V. If the pull-ups are implemented as discrete resistors, or resistor packs, a value of 470k should be used. SOC internal pull-up / current source features may be used instead of external resistors.

All GPIO pins shall be capable of generating interrupts. The interrupt characteristics (edge or level sensitivity, polarity) are generally configurable in the SOC register set.

2.19.1 GPIO Signals

Table 57: GPIO Signals, Pin Types, and Descriptions

Signal	Pin#	Description	I/O	Note
GPIO0 / CAM0_PWR# GPIO1 / CAM1_PWR# GPIO2 / CAM0_RST# GPIO3 / CAM1_RST# GPIO4 / HDA_RST# GPIO5 / PWM_OUT	P108 P109 P110 P111 P112 P113	General Purpose Outputs for system specific usage. Carrier Board: Connect to GPO[0:5] N/C if not used	I/O CMOS Runtime 1.8V	1,2
GPIO6 / TACHIN GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13	P114 P115 P116 P117 P118 P119 S142 S123	General Purpose Input for system specific usage. These signals have pull up 10K Ω on the module.. Carrier Board: Connect to GPI[6:13] N/C if not used	I/O CMOS Runtime 1.8V	1,2

Note:

1. SMARC Spec also allows for SoC integrated Pull-Ups, these can be ≥ 20k. Max 2.2k PD should be implemented on Carrier if a low level needs to be ensured.

2 .GPIO[0:3] are GPIO function. GPIO[4:6] are option function.

2.19.2 GPIO Signal Routing Guidelines

NA

2.19.3 GPIO Signal Trace Length Guidelines

NA

2.20 Miscellaneous Signals

The input pins listed in this table are all active low and are meant to be driven by OD (open drain) devices on the Carrier. The Carrier either floats the line or drives it to GND. No Carrier pull-ups are needed. The pull-up functions are performed on the Module. The voltage rail that these lines are pulled to on the Module varies, depending on the design.

Switches to GND ***may*** be used instead of OD drivers for lines such as PWR_BTN# and RESET_IN#.

2.20.1 Miscellaneous Signals

Table 58: Miscellaneous Signal Definitions

Signal	Pin#	Description	I/O	Note
WDT_TIME_OUT#	S145	Watch-Dog-Timer Output Carrier Board: Connect to Watchdog trigger input. N/C if not used	O CMOS Runtime 1.8V	
VIN_PWR_BAD#	S150	Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) shall not be enabled while this signal is held low by the Carrier. This signal has pull up 10K Ω to 5V on Module. Driven by OD part on Carrier. Carrier Board: Connect to VIN_PWR_BAD# circuit. N/C if not used	I OD CMOS VDD_IN	
CARRIER_PWR_ON	S154	Carrier board circuits (apart from power management and power path circuits) ***should not*** be powered up until the Module asserts the CARRIER_PWR_ON signal. On x86 designs this pin ***should*** utilize the SUS_S5# signal, but then it ***shall*** maintain still the CARRIER_PWR_ON functionality to avoid back driving. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Carrier Board: Connect to CARRIER_PWR_ON circuit. N/C if not used	O CMOS Standby 1.8V	

Signal	Pin#	Description	I/O	Note
CARRIER_STBY#	S153	The Module ***shall*** drive this signal low when the system is in a standby power state. On x86 designs this pin ***should*** utilize the SUS_S3# signal. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Carrier Board: N/C if not used	O CMOS Standby 1.8V	
RESET_OUT#	P126	General purpose reset output to Carrier board. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Carrier Board: N/C if not used	O CMOS Standby 1.8V	
RESET_IN#	P127	Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise. Pulled up on Module. Driven by OD part on Carrier. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Carrier Board: N/C if not used	I OD CMOS Standby 1.8V	
POWER_BTN#	P128	Power-button input from Carrier board. Carrier to float the line in in-active state. Active low, level sensitive. ***Should*** be de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Carrier Board: Connect to Power button. N/C if not used	I OD CMOS Standby 1.8V	

Signal	Pin#	Description	I/O	Note
SLEEP#	S149	Sleep indicator from Carrier board. ***May*** be sourced from user Sleep button or Carrier logic. Carrier to float the line in in-active state. Active low, level sensitive. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: Connect to Sleep button. N/C if not used	I OD CMOS Standby 1.8V	
LID#	S148	Lid open/close indication to Module. Low indicates lid closure (which system ***may*** use to initiate a sleep state). Carrier to float the line in in-active state. Active low, level sensitive. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: Connect to LID button. N/C if not used	I OD CMOS Standby 1.8V	
BATLOW#	S156	Battery low indication to Module. Carrier to float the line in in-active state. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: Connect to BATLOW# of Smart Battery. N/C if not used.	I OD CMOS Standby/Sleep 1.8V	
CHARGING#	S151	Held low by Carrier during battery charging. Carrier to float the line when charge is complete. This signal has pull up 10K Ω to 1.8V_DUAL on Module.. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby/Sleep 1.8V	
CHARGER_ PRSNT#	S152	Held low by Carrier if DC input for battery charger is present. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby/Sleep 1.8V	

Signal	Pin#	Description	I/O	Note
TEST#	S157	Held low by Carrier to invoke Module vendor specific test function(s). This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby/Sleep 1.8V	1

Note:

1. The Module TEST# pin (pin S157) should normally be left not connected. If pulled low, then Module specific test function(s) may be enabled.

2.20.1.1 Watchdog Control Signals

The Watchdog on SMARC modules can be initialized and controlled by the API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more details about EAPI, refer to the SMARC specification and Advantech's EAPI Programmers Guide.

In addition to the software trigger available via EAPI, the Watchdog on a SMARC module can be hardware-triggered by an external control circuitry. When generating a low level pulse on the Advantech's *'WDTRIG#'* (Watchdog trigger signal) signal, the Watchdog timer will be reset and restarted.

If the Watchdog timer has expired without a software or hardware trigger occurrence, the SMARC module will signal this with a high level output on the *'WDOUT'* (Watchdog event indicator) signal.

2.20.2 Miscellaneous Signals Routing Guidelines

NA

2.20.3 Miscellaneous Signals Trace Length Guidelines

NA

2.21 Fan Control Implementation

2.21.1 Fan Control Interface

SMARC modules provide additional support for fan speed control through the use of two signals named *'FAN_TACHOIN'* and *'FAN_PWMOUT'*. In order to easily implement fan speed control in customer specific application software, there is a software API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more information about EAPI, refer to the SMARC specification and the Advantech's EAPI Programmers Guide.

Table 59: Fan Control Signal Definitions

Signal	Pin#	Description	I/O	Note
PWM_OUT / GPIO5	P113	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output. Carrier Board: 4-Wire PWM Fan - Connect 3.3V to 5V level shift to fan connector pin 4 CONTROL with bypass 470pF to GND. 3-Wire PWM Fan - Connect 3.3V to 12V level shift to fan connector pin 2 PWR with bypass 470pF/10uF to GND. N/C if not used.	O CMOS Runtime 1.8V	1
TACHIN / GPIO6	P114	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input. Carrier Board: 4-Wire PWM Fan - Connect to diode anode and diode cathode connects to fan connector pin 3 SENSE with bypass 470pF to GND. 3-Wire PWM Fan - Connect to diode anode and diode cathode connects to fan connector pin 3 TACHO with bypass 470pF to GND. N/C if not used.	I CMOS Runtime 1.8V	2

Note:

1. Default is PWM_OUT, GPIO5 is option function.
2. Default is TACHIN, GPIO6 is option function.

2.21.2 Fan Control Signals Routing Guidelines

NA

2.21.3 Fan Control Signals Trace Length Guidelines

NA

2.22 Boot Select

2.22.1 Boot Definittions

Most SOCs used on SMARC Modules have the following attributes:

1) An internal ROM exists. The internal ROM code is executed after the SOC comes out of reset. This ROM code is provided by the silicon vendor and is generally not available or visible to users.

2) A set of SOC strap pins is used to select what SOC physical device interface (SD Card, SPI, eMMC, etc.) will be used for the second – stage boot process (also known as BCT or Boot Configuration Table boot). There is no commonality between various SOCs as to how the strap pins are defined.

3) The SOC pin configuration is very flexible – most SOC pins can be used for several functions, and the SMARC Module designer must choose a pin configuration that works for the design at hand. The SOC pin configuration is set by a Boot Configuration Table that is read out from the external boot media (SD Card, SPI, eMMC, etc.).

There are several stages in the boot process:

1) Internal SOC ROM execution

2) second stage boot, from non-volatile memory external to the SOC: BCT is loaded and various other system parameters are set

3) Operating System load

The Operating System load may occur from the same memory as the second stage BCT boot, or the second stage code may pass the Operating System load off to another device, such as a USB drive or SATA drive.

2.22.2 Boot Selection Signals

Three Module pins allow the Carrier board user to select from eight possible boot devices. Three are Module devices, and four are Carrier devices, and one is a remote device. The pins ***shall*** be weakly pulled up on the Module and the pin states decoded by Module logic. The Carrier ***shall*** either leave the Module pin Not Connected ("Float" in the table below) or ***shall*** pull the pin to GND, per the second table below.

A "Force Recovery" provision exists, per the pin description below.

Table 60: Boot Selection Signals Descriptions

Signal	Pin#	Description	I/O	Note
BOOT_SEL0#	P123	Input straps determine the Module boot device. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby 1.8V	1
BOOT_SEL1#	P124	Input straps determine the Module boot device. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby 1.8V	1
BOOT_SEL2#	P125	Input straps determine the Module boot device. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby 1.8V	
FORCE_RECOV#	S155	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked. For SOCs that do not implement a USB based Force Recovery functions, then a low on the Module FORCE_RECOV# pin ***may*** invoke the SOC native Force Recovery mode – such as over a Serial Port. For x86 systems this signal ***may*** be used to load BIOS defaults. This signal has pull up 10K Ω to 1.8V_DUAL on Module. Driven by OD part on Carrier. Carrier Board: N/C if not used.	I OD CMOS Standby 1.8V	2

Note:

1. SOM-2532 is NC pins.
2. No function at SOM-2532.

2.22.3 SMARC Boot Selection Pin

The SMARC Hardware Specification defines 3 SMARC pins, designated BOOT_SEL0# through BOOT_SEL2#, that may be used to tell the Module what physical device to do a BCT boot from. The SMARC BOOT_SELx# pins serve to abstract the SOC – dependent strap definitions into a common SMARC definition. The table below is reproduced from the SMARC Hardware Specification document.

Table 61: Boot Select Pins

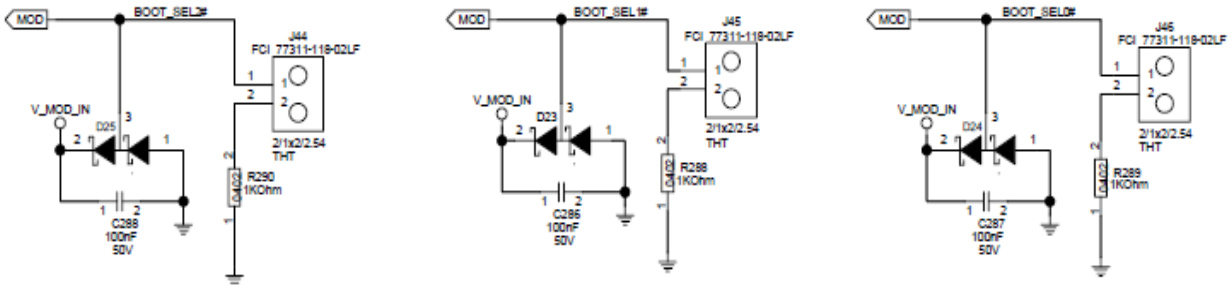
	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	GND	Carrier SATA
1	GND	GND	Float	Carrier SD Card
2	GND	Float	GND	Carrier eSPI (CS0#)
3	GND	Float	Float	Carrier SPI (CS0#)
4	Float	GND	GND	Module device (NAND, NOR) – vendor specific
5	Float	GND	Float	Remote boot (GBE, serial) – vendor specific
6	Float	Float	GND	Module eMMC Flash
7	Float	Float	Float	Module SPI

Note:

The boot sources shown above are Module options, and ***may not*** be available on all Module designs. The definition of “boot” is left to the Module designer. Some designs ***may*** literally implement some or all of the table above, such that the first off-SOC code fetches come from the devices listed above. Alternatively, some designs ***may*** always fetch the first few off-SOC instructions from a fixed device, likely a SPI Flash EEPROM, and then re-direct the execution to another device per the table above.

The Module BOOT_SELx# pins may be set by jumpers on the Carrier Board, as shown in the figure below. The diodes and capacitors are for ESD protection, as the jumpers may experience ESD events. Alternatively, the BOOT_SELx# pins can be set by low value option resistors to GND on the Carrier. The resistors are either installed (for a GND connection) or not installed, per the table above.

Figure 36: Boot Selection Jumpers



2.23 IO Levels

2.23.1 Default I/O 1.8V

In the interest of minimizing system power, the majority of SMARC I/O is at a 1.8V level. Most SOCs used for SMARC systems are optimized for 1.8V I/O. Recall that the power required to charge and discharge the pin capacitance of a target IC is proportional to the **square** of the I/O voltage.

2.23.2 Signals at 3.3V

A few SMARC interfaces run at 3.3V to interface with industry standard devices on the Carrier that run at 3.3V. Such interfaces include the SD Card signals (SDIO_ prefix); the USB[0:5]_EN_OC# signals; the USB[0,3]_OTG_ID signals; the PCIE support signals (x = A, B, C; support includes PCIE_[A:C]_CKREQ# and PCIE_[A:C]_RST#); the PCIE_WAKE# signal; the SATA_ACT# signal and the GBE[0:1]_LINK_100#, GBE[0:1]_LINK_1000#, GBE[0:1]_LINK_ACT# signals.

2.23.3 Signals at 5V

The USB[0,3]_VBUS_DET signals are 5V tolerant.

2.24 Power and GND

Table 62: Power and GND

Signal	Description	I/O	Note
VDD_IN	Module power input voltage - 3.0V min to 5.25V max	Power In	1
GND	Module signal and power return, and GND reference	Ground	
VDD_RTC (Pin S147)	Low current RTC circuit backup power – 3.0V nominal *May* be sourced from a Carrier based Lithium cell or Super Cap.	Power In Power Out (when charging a Super Cap)	

Note:

1.SOM-2532 supports 3V~5V input.

3 Power

3.1 Input Voltage / Main Power Rail

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector.

A Module ***shall*** withstand an indefinite exposure to an applied VDD_IN that ***may*** vary over the 3.0V to 5.25V range, without damage.

A Module ***should*** operate over the entire VDD_IN range of 3.0V to 5.25V.

Modules that use higher wattage SOCs ***may*** be designed to operate with a fixed 5V supply (4.75V to 5.25V).

Modules that are designed for rock-bottom cost and that use low power SOCs ***may*** be designed to operate with a fixed 3.3V supply (3.1V to 3.4V). They ***shall not*** be damaged in any way by exposure to the allowable VDD_IN range of 3.0 to 5.25V.

Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage of 3.0V, this would allow up to 15W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 9W ***may*** be brought in at 3.0V.

If the fixed 5V input option is used, then 25W ***may*** be brought in over the 10 power pins (no de-rating). With a 40% connector de-rating, 15W are allowed to be brought in at 5V

As a practical matter, X86 designs are expected to be in the 5W to 12W range, depending on the CPU SKU.

Note: SOM-2532 supports the VDD_IN range of 3V to 5.25V.

3.2 No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current (optional) RTC voltage rail. All Module operating and standby power comes from the single set of VDD_IN pins. This suits battery power sources well, and is also easy to use with non-battery sources.

3.3 RTC Voltage Rail

RTC backup power ***may*** brought in on the VDD_RTC rail. The RTC consumption is typically 15 microA or less.

The allowable VDD_RTC voltage range ***shall*** be 2.0V to 3.25V. The VDD_RTC rail ***may*** be sourced from a Carrier based Lithium cell or Super Cap, or it ***may*** be left open if the RTC backup functions are not required.

The Module ***shall*** be able to boot without an external VDD_RTC voltage source.

Important: Lithium cells must be protected against charging by reverse currents, with a series Schottky diode and resistor. It is impractical to have the series diode on the Module, as this complicates the use of Super Caps (they need to be charged, over the Module VDD_RTC pin).

Lithium cells, if used, ***shall*** be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module VDD_RTC side.

Note that if a Super cap is used, current ***may*** flow out of the Module VDD_RTC rail to charge the Super Cap.

3.3.1 RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the carrier board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current it should be measured when the complete system is disconnected from AC power.

The RTC power plane is normally ored with the 3V3 Voltage on the module, so it may not be necessary to perform this on the carrier board. Please consult Advantech's documentation.

3.4 Power Sequencing

The Module signal CARRIER_PWR_ON exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits should not be powered until the Module asserts the CARRIER_PWR_ON signal as a high. Module hardware should assert CARRIER_PWR_ON when all Module supplies necessary for Module booting are up. The Module should continue to assert signal CARRIER_RESET_OUT# after the release of CARRIER_PWR_ON, for a period sufficient (100ms to 500ms) to allow Carrier power circuits to come up. Only one single supply voltage rail is used for the module. There are no timing relations between this module supply rail VDD_IN and the optional VDD_RTC.

Figure 37: Power On Sequencing

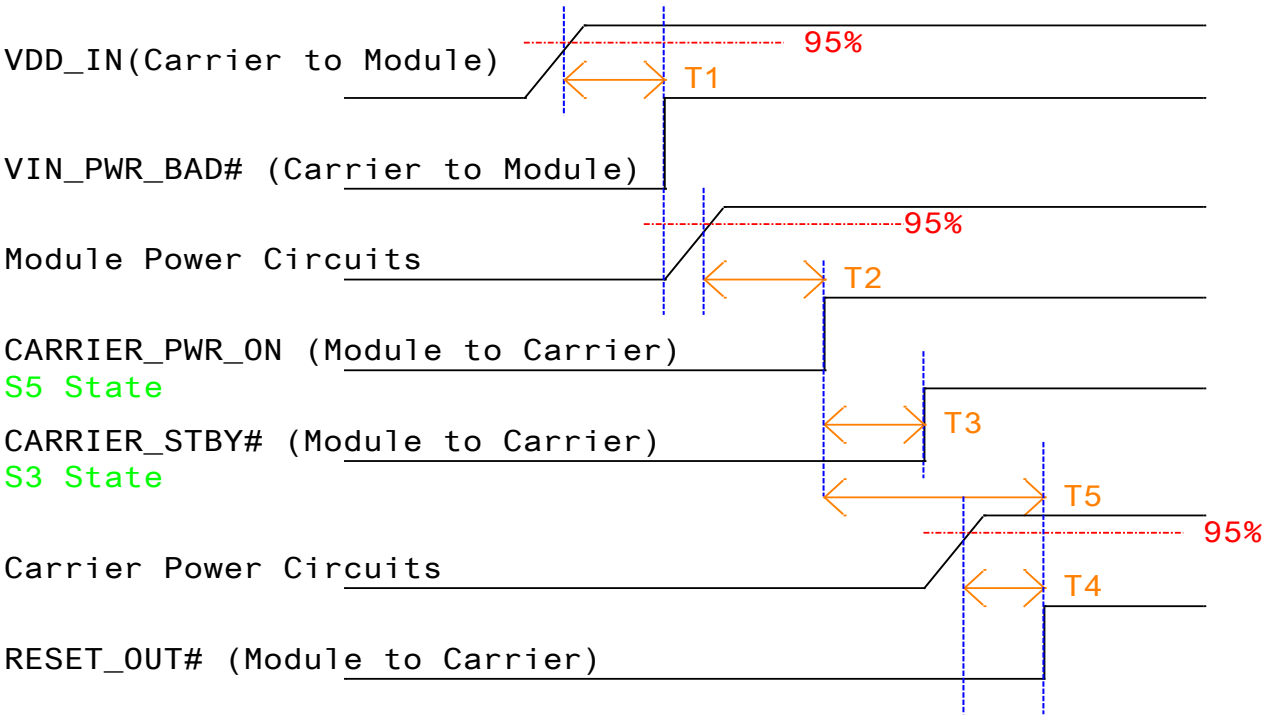


Table 63: Power Management Timings

Sym	Description	Min	Max
T1	VDD_IN stable to VIN_PWR_BAD# rise	0 ms	
T2	Module supplies necessary for Module booting are up to CARRIER_PWR_ON rise	0 ms	
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	0 ms	
T4	Carrier power circuits are up to RESET_OUT# rise	0 ms	
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 ms	500ms

Note:

3.4.1 x86 Power Management

The power management of x86 systems typically utilizes the signals SUS_S5# and SUS_S3# to indicate the sleep states and to control the ATX power supply. SMARC supports only single voltage supply and no ATX power supply; therefore these signals can only be used to indicate, if the module is in one of the sleep states.

For S3 state the SMARC signal CARRIER_STBY# should be utilized
For S5 states the SMARC signal CARRIER_PWR_ON should be utilized, but the CARRIER_PWR_ON functionality to avoid back driving shall be still maintained.

SUS_S3# CPU Signal
Indicates system is in Suspend to RAM state.
ACPI S3 State "Suspend to RAM"
The CPU is not executing instructions, is not ready to execute instructions, does not maintain its registers and does not maintain cache. The OS must flush dirty pages from the cache when S3 is entered. Devices able to support S3 and are enabled for resuming, may resume the system. Power supply state is off, system RAM is refreshed. External peripherals (keyboard, mouse) may or may not be able to resume the system, depending on their host controller.

SUS_S5# CPU Signal
Indicates system is in Soft Off state.
ACPI S5 State "Soft-Off"
All hardware is in the off state and maintains no context. CMOS is maintained, as in S4. The power supply is in off state. Power may be mechanically removed without ill effect.

3.5 System Power Domains

It is useful to describe an SMARC system as being divided into a hierarchy of three power domains:

1) Battery Charger power domain
2) SMARC Module power domain
3) Carrier Circuits power domain

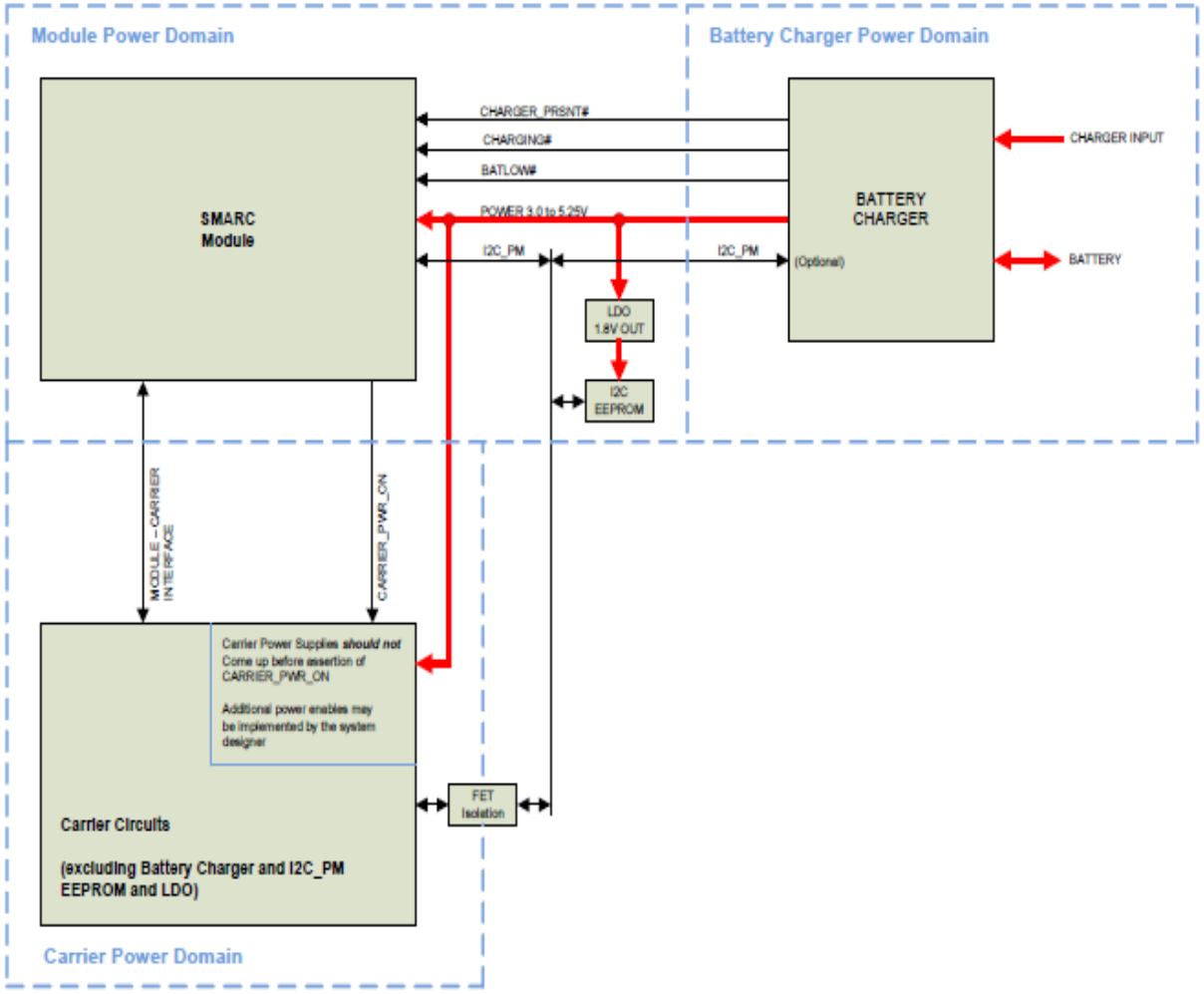
The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits *may* include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.

The SMARC Module domain includes the SMARC module and *may* include a serial EEPROM on the Carrier, connected to the I2C_PM I2C bus in the Module power domain, allowing Module software to read Carrier board parameters.

The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they *may* be mounted on the Carrier).

This is illustrated in the Figure 38 below.

Figure 38: System Power Domains



4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 64: Absolute Maximum Ratings

SOM-2532		MIN	MAX	UNIT
Power	VIN	3	5.25 (5+5%)	V
	VSB	4.75 (5-5%)	5.25 (5+5%)	V
	RTC Battery	2.3	3.3	V

4.2. DC Characteristics

Table 65: Input Power Consumption of 5V

Power Plane	Maximum Power Consumption				
Symbol	S0		S3	S5	G3
+VIN (+5V)	TAT CPU+GPU100%				
	Idle				
+V5SB_CB					
RTC Battery					

4.3. Inrush Current

Table 66: Inrush Current

Power Plane	Maximum	
Symbol	G3 to S5	S5 to S0
+V5SB_CB		
+VIN (+5V)		

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